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CMOS analog transmission gate design

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CMOS ANALOG TRANSMISSION GATE DESIGN

by

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Approved by:

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ABSTRACT

CMOS technology has provided an integrated circuit equivalent for the conventional electromechanical switch: the transmission gate. CMOS analog transmission gates degrade signals passed through them with noise due to gate clock feedthrough transients. A SPICE parameter model for the Eastman Kodak CMOS process has been developed and timing requirements for feedthrough cancellation in typically structured transmission gate devices have been studied. An alternate device structure for improved performance is proposed.

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LIST OF SYMBOLS

Symbol	Definition, units
N_{sub}	Substrate (or tub) dopant concentration, atoms/cm^3
n_i	Intrinsic carrier concentration, atoms/cm^3
ε	Permittivity, Farads/meter
t	Thickness, meters
ϕ_f	Fermi potential
u	Micron (10^{-6} meters)
μ	Mobility, centimeters^2/Volt-second
W	Device channel width, meters
L	Device channel length, meters
γ	Body effect factor
λ	Channel length modulation factor
V_G	Gate voltage, Volts
V_D	Drain voltage, Volts
V_S	Source voltage, Volts
V_{in}	Input (signal) voltage, Volts
V_T	Threshold voltage, Volts
V_{T0}	Zero bias threshold voltage, Volts
Ω	Resistance, Ohms
K	Boltzmann's constant, 1.38*10^{23} Joules/°Kelvin
k	Kilo (10^3)
T	Temperature, °Kelvin
q	Charge, Coulombs
β	MOSFET gain factor

INTRODUCTION

CMOS technology has provided an integrated circuit equivalent for the conventional electromechanical switch: the transmission gate. The use of transmission gates can lead to more efficient layouts and can reduce logic, thus reducing die size and improving circuit speed. This gate is often used to multiplex signals into analog-to-digital converters, to tristate lines, and to isolate sections of circuits. The transmission gate has become a major building block for logic design, data filtering, data conversion, and other signal processing circuits.

Transmission gates can benefit many functions, but they have limitations which are a result of their resistive nature. They have no drive capability of their own. An ideal semiconductor switch would have infinite off-resistance, zero on-resistance, no leakage, no parasitic capacitance, and would consume no power. Since the transmission gate is not ideal, the integrated circuit designer must optimize performance by using the switch configuration that most closely meets circuit requirements. In this work, emphasis is placed on transmission gates which rapidly switch small signals with minimum signal distortion. Further, a transmission gate configuration suitable for the CMOS process at the Eastman Kodak Company is sought.

BACKGROUND AND THEORY

The simplest switch implementation is a pass transistor, such as the Field Effect Transistor (FET) shown in figure 1. FET switches can be used to transfer voltage to nodes with large impedances, to switch currents between two alternative loops, or to transfer charge, as with switched capacitor filters, where charge is conserved.

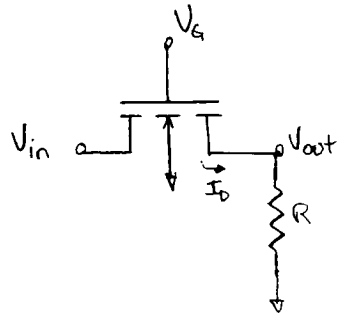


Figure 1. Simple FET Switch

The signal at the output, V_{out},

$$V_{out} = I_D R \tag{1}$$

depends on the current through the device, I_D,

$$I_{Dsat} = \beta(V_{GS} - V_T)^2 \tag{2a}$$

where β is composed of the fabrication and geometrical parameters,

$$\beta = \mu\varepsilon_{ox}W \,/\, 2t_{ox}L(\,1 + \lambda V_{DS}) \tag{2b}$$

With the appropriate biases, the voltage on the gate of the device, V_{GS}, controls the blockage or passage of signals.

This switch implementation has three important limitations. The first is a result of the requirement for conduction: the voltage

on the gate must exceed that of the source by the threshold voltage. This limits the voltage swing of signals passing through the device for a fixed gate voltage. An FET in the conducting state also acts as a nonlinear resistor. Its on-resistance is strongly dependent on temperature and signal voltage, limiting its applicability. The third limitation arises from the gate-to-channel capacitance. The charge in the channel is controlled by the gate-to-source voltage, V_{GS}.

$$Q_{sat\ ch} = -C'_{ox}WL(V_{GS} - V_D/2 - V_T) \qquad (3)$$

When an n-channel device is to be switched from the conducting state to the nonconducting state, the gate voltage is decreased and the charge in the channel diminishes by the relation given in equation (3). The electrons can diffuse in all directions, but will tend to follow the low potential paths toward the source and drain. The part of the channel charge that follows the potential toward the output node becomes indistinguishable from the signal. The result is a gate clock ghost at the output. For small signal voltage levels, this can be a significant source of noise. Low frequency circuits can deal with this by slowing the gate voltage ramps, and by sampling the signal after the gate feedthrough has settled out. However, for high frequency operation an abrupt change in the gate voltage is required to rapidly switch the state of the device and time may not available to delay sampling. Thus small high frequency signals can be lost in the gating feedthrough.

A reduction of the feedthrough error can be realized with the

configuration shown in figure 2.1 Using this connection scheme, no current flows in the additional transistor, but it does have an inverted channel in the conducting state. When the conduction state is switched, the feedthrough transient from the p-channel (holes) will ideally cancel the transient from the n-channel (electrons). Thus, complementary transistors with gate voltage clocks of opposite phase can reduce feedthrough noise. The sacrifice for this improvement is additional area for the extra FET and the increasingly complex gate control circuitry.

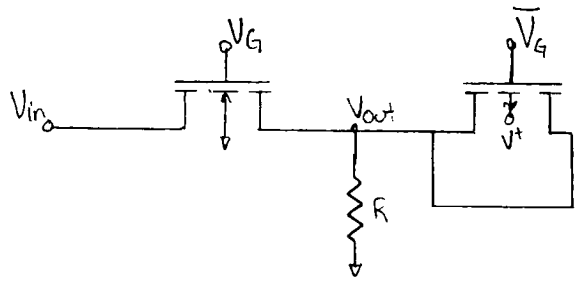


Figure 2. Improved Switch

The appropriate geometry for the additional transistor can be determined from equation (3). Both the source and drain of the dummy transistor are connected to the output node, so its transient will consist of virtually all of the channel charge. The total amount of channel charge will depend on the level of V_{GS}. If V_G and $\overline{V_G}$ are chosen so that each transistor develops the same amount of channel charge, then the dummy FET should be scaled so that its area is half that of the switch FET.

This structure is still limited to signal swings which do not fall below the on-state gate voltage less the device threshold voltage. An additional problem is introduced due to the body effect. This switch is illustrated in cross-section in figure 3. In the CMOS process shown, p-channel FET's are built in an n-type tub or well. As the input signal voltage changes with respect to the n-well voltage, the n-well-to-input-diffusion depletion will change. This shift in depletion charge must be offset to turn the transistor on. The effect can be represented as an increase in threshold voltage. In unidirectional circuits, the V_T shift due to the body effect can be minimized by tying the tub to the source diffusion. This will insure that no additional voltage difference exists between the tub and input diffusion with signal level changes.

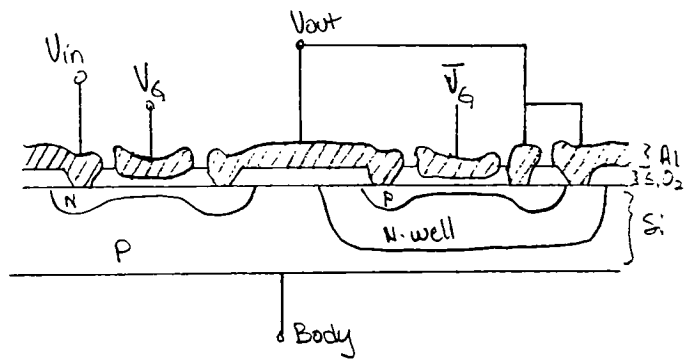


Figure 3. Improved Switch Cross-Section

A further improvement over the simple switch consists of complementary FET's connected in parallel, as shown in figure 4.

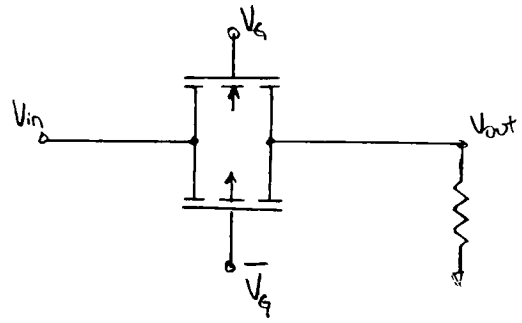


Figure 4. Schematic Transmission Gate

There is no longer a limitation on the voltage swing of the signal because one of the transistors can always conduct. Consider matched FET's with ±2v threshold voltages, and ±5v gate voltages.

	n-channel	p-channel
V_{in}	$[(V_G - V_{in}) > V_T]$?	$[(V_G - V_{in}) < V_T]$?
-10v	[5 - (-10) > 2] = on	[-5 - (-10) < (-2)] = off
-5v	[5 - (-5) > 2] = on	[-5 - (-5) < (-2)] = off
0v	[5 - 0 > 2] = on	[-5 - 0 < (-2)] = on
+5v	[5 - (+5) > 2] = off	[-5 - (+5) < (-2)] = on
+10v	[5 - (+10) > 2] = off	[-5 - (+10) < (-2)] = on

Negative input signals are primarily conducted through the n-channel device and positive signals are primarily conducted through the p-channel device. The on-resistance is greatest at the points when both transistors are partially conducting; otherwise the on-resistance of the conducting FET dominates. Once the gate voltage levels are known, the transistor scaling can be determined using equation (3). With this structure, the transistors should be scaled

so their gate-to-channel capacitances are equal.

The problem of gating feedthrough can also be ideally eliminated with complementary (opposite phase) gate voltage clocks. To minimize feedthrough in critical circuits, the gate clocks must be adjustable. This is necessary to insure that the feedthrough transients of holes and electrons reach the output node at the same moment for accurate cancellation. The lower mobility of holes requires that the p-channel device be turned off before the n-channel device and with a steeper ramp. Further, the mobilities and the threshold voltages will shift with temperature and signal level. This presents a nontrivial set of operational requirements.

For some applications, a solution which addresses these concerns and also tracks with processing variations includes a clock-phase control circuit.[2] The control circuit, as shown in figure 5, employs an extra transmission gate identical to those it controls. The integrated gate feedthrough signal shortens the on-period of the p-channel transistor in the other transmission gates. This technique is most applicable in circuits which are clocked repeatedly while processing a static signal, such as with A/D converters.

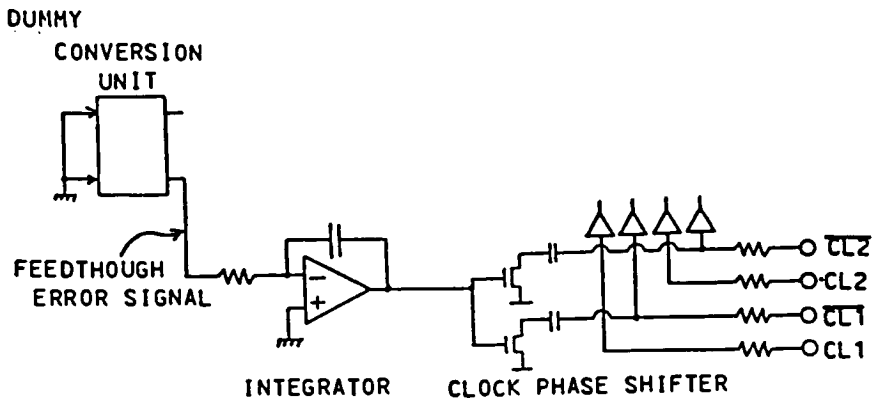


Figure 5. Clock-Phase Controller

In rectangular FET's, the channel charge splits symmetrically when the device changes state. A potential improvement can be had by either asymmetrically doping the channel region or modifying the gate geometry. The improvement arises from the asymmetric distribution of channel charge and provides a more conducive path back toward the signal input, rather than toward the output. In one device, asymmetric wedging from source to drain has been maximized by making the source very large and the drain very small. The result is a semi-circular transistor, as shown in figure 6. It has been shown to reduce the error charge by 60% over the equivalent rectangular device.[3]

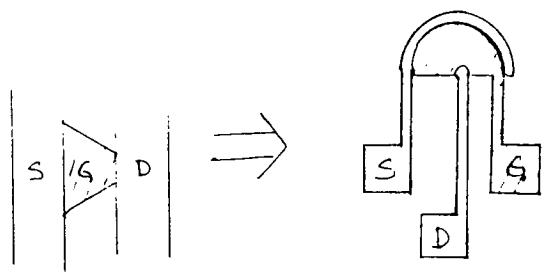


Figure 6. Circular Pass Transistor

Dependence on temperature and signal voltage still exists in all of these configurations. Figure 7, by G. Bouhasin, illustrates this dependence for the standard configuration given in figure 4.4 Transmission gates exhibit a nonlinear impedance as the signal voltage is varied. The nonlinearity is more pronounced with lower gate supply voltages.

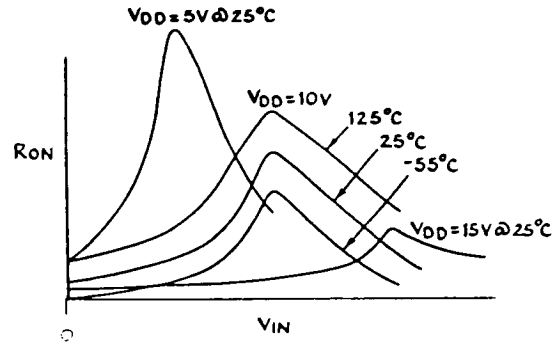


Figure 7. R_{on} vs. V_{in}

CMOS switches exhibit less current leakage than other fabrication technologies.[5] However, some leakage will occur and it will depend of the polarity of V_S. When V_S is negative, the p-channel device may leak; when V_S is positive, the n-channel device may leak. Figure 8 illustrates the off-state leakage model for the transmission gate diagrammed in figure 4.

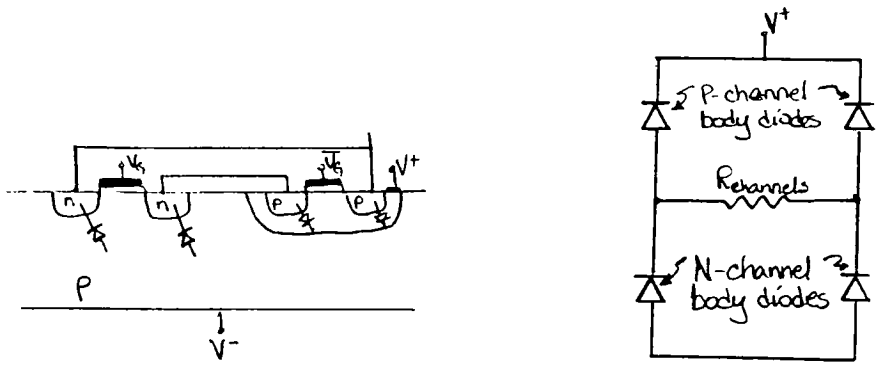


Figure 8. Transmission Gate Leakage Model

A number of designers have developed application techniques to circumvent the temperature and impedance limitations.[6-13] Such techniques include connecting an always-on transmission gate in a feedback loop for temperature and gain compensation, and buffering with a unity gain stage which provides a high series impedance, reducing the effect of the impedance nonlinearity. In situations where a low on-resistance is required, bipolar, DMOS, or another pair of CMOS transistors are incorporated.[13-15] One such configuration is shown in figure 9.

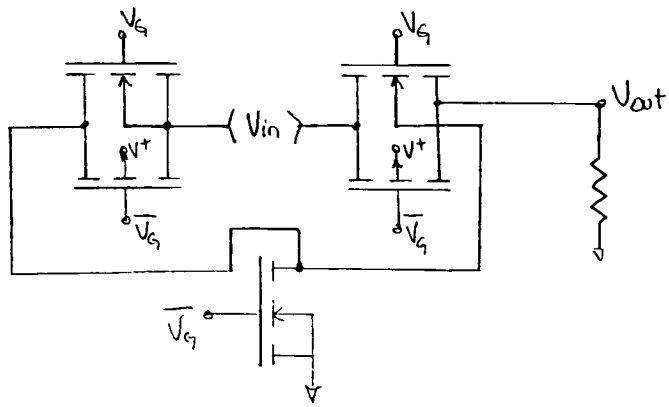


Figure 9. Alternative Transmission Gate

To reduce the on-resistance, a second pair of transistors has been added in parallel. Another FET insures that the structure will be

held in cutoff since it is more likely to leak. The n-channel device built in the p-well may turn off early for low values of V_{in}, a result of the body effect. To minimize this, the p-well is connected to V_{in} in the on-state; to reduce the sensitivity to leakage in the off-state, it is connected to V^-.[4,16]

A discussion of the structures examined in this study will now be presented.

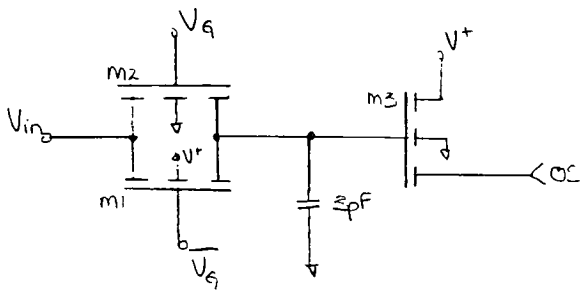
DISCUSSION

The Eastman Kodak CMOS process is based on p-type wafers, hence n-channel devices are fabricated in the bulk and the p-channel devices are built in an n-well. In this project, several types of devices previously processed at Kodak were examined. A test structure containing transmission gates was evaluated to gain understanding of the problem. Another test structure containing transistors with modified gate and channel geometries was also evaluated. Finally, tests were performed on both long and shorter channel length FET's to gather data from which CMOS modeling parameters could be extracted. The first part of the discussion deals with the transmission gate test structure. It is followed by a discussion of the modified transistors and then the CMOS process characterization tests.

TRANSMISSION GATE TEST STRUCTURE

The transmission gate test structure, shown in figure 10, consists of parallel n- and p-channel FET's connected to a holding capacitor and an FET follower. The same test structure was laid out with three different p-channel geometries (T12, T13, T14) to offset the variation in source-to-n-well depletion due to the body effect. Since the difference between the source and n-well voltages modulates the width of the depletion region symmetrically around the source, a larger source serves to reduce the net modulation at the source-to-channel interface. The result is a transistor which

exhibits less shift in V_T with V_{in}.



Test Structure	M1 W/L	M2 W/L	M3 W/L
T12	40u/10u	40u/10u	120u/10u
T13	44u/10u	"	"
T14	50u/10u	"	"

Figure 10. Transmission Gate Test Structure

The test structure was first evaluated for the change in on-resistance with signal voltage, V_{in}. As previously discussed, n-channel devices conduct primarily for negative signal voltages and p-channel devices conduct primarily for positive signal voltages. For this test, V_{in} was swept from -5 to +20 volts with V_G of ±5 volts. The threshold voltages for the n- and p-channel devices were .6v and -1.0v, respectively. The n-well was tied to V_{in} and the substrate was biased at -7 volts. The n- and p-channel resistances are shown individually in figure 11. The curves follow typical behavior, as shown previously in figure 7, until V_{in} reaches -.7 volt. At this point, it is probable that another junction becomes forward biased. Information is not available for exact determination.

Next, the test structure was evaluated for the dependence of R_{on} with V_G. Over a standard working range of 0 to 10 volts, R_{on} varies considerably. This test was performed for gate voltages of

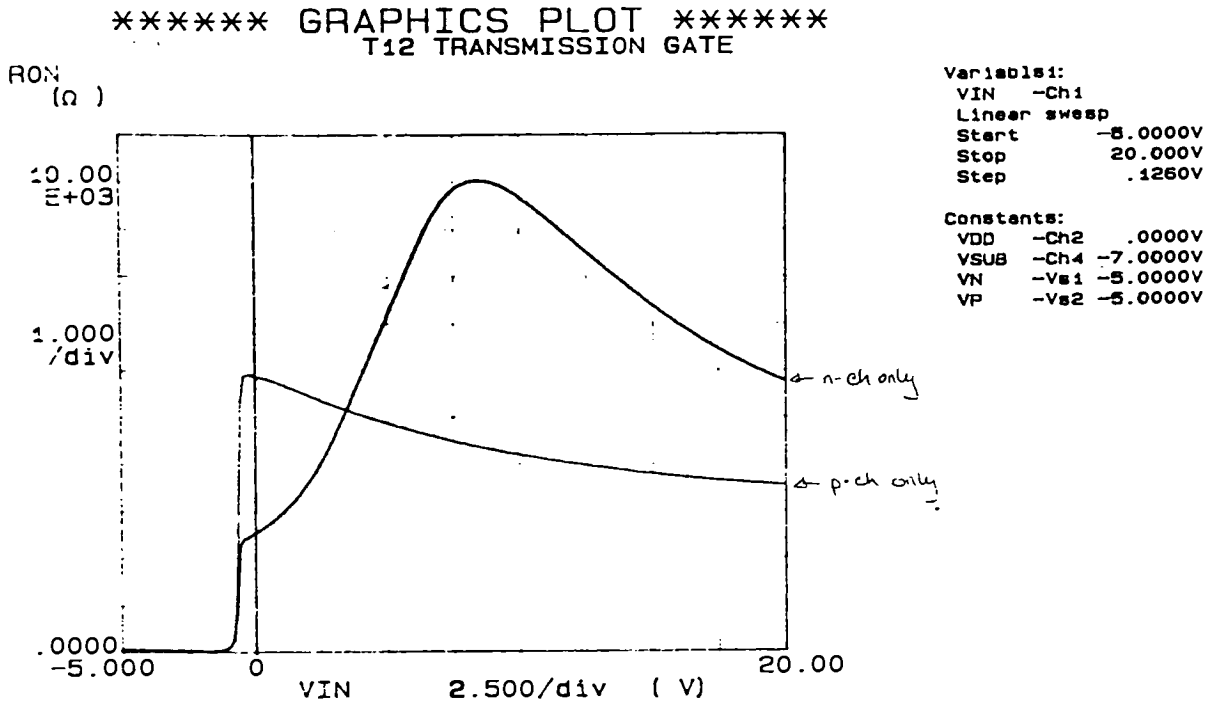


Figure 11. P- and n-channel R_{on} vs. V_{in}

RON (Ω) = (VDD-VIN)/IDD

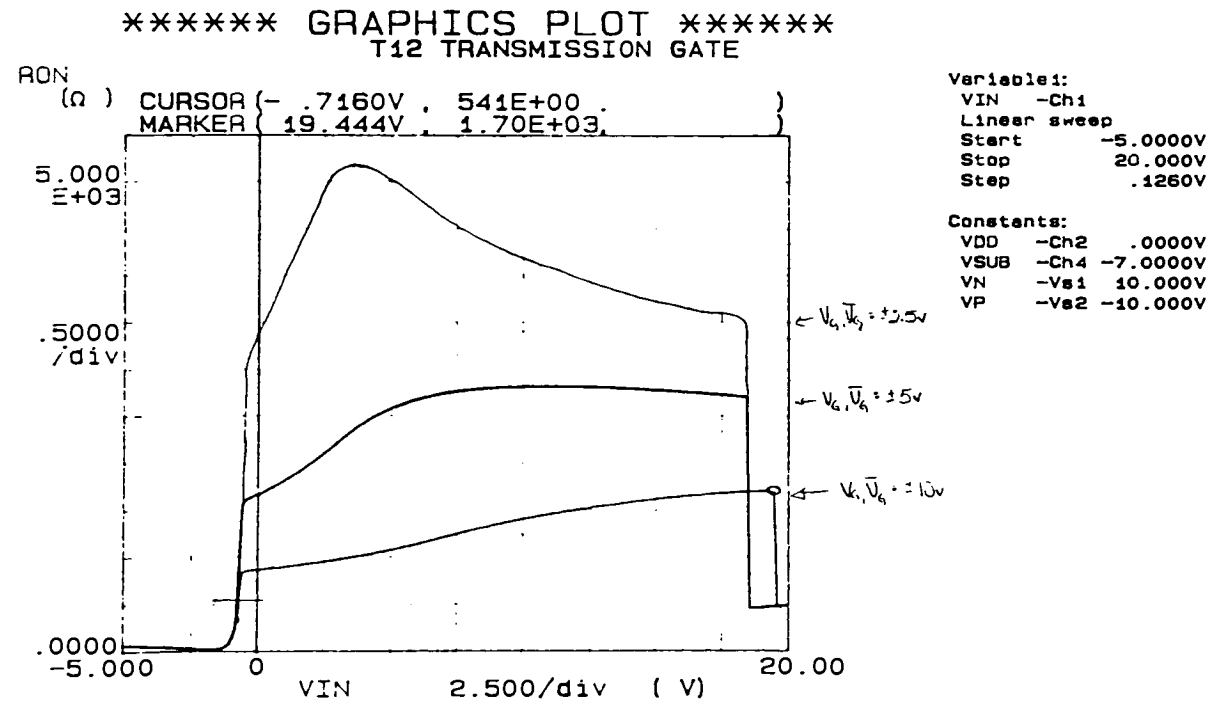


Figure 12. Transmission Gate R_{on} vs. V_{in} vs. V_G

RON (Ω) = (VDD-VIN)/IDD

10v. 5v, and 2.5 volts. The use of higher gate supply voltages reduces the variation in R_{on} and also increases the functional range of the transmission gate. Typical curves of the resistance variation with gate and signal voltage are shown in figure 12. The data are summarized below.

Device	Gate Voltages	Resistance Min	Max	Change
T14	±10	.75 KΩ	1.4 KΩ	.65 KΩ
T14	±5	1.7 KΩ	2.8 KΩ	1.1 KΩ
T14	±2.5	3.4 KΩ	5.2 KΩ	1.8 KΩ

Table 1. Resistance variation with Gate Voltage

The effect of device size on R_{on} was examined. An increase in the p-channel device width decreases R_{on}. For -7v gate voltages, the resistance decreases approximately 35 Ω/u additional width.

Device	Gate Voltage	P-Width	Resistance, maximum
T12	-7v	40u	2.6 KΩ
T13	-7v	44u	2.45 KΩ
T14	-7v	50u	2.25 KΩ

Table 2. Resistance Variation with Device Width

Also of interest is the gating feedthrough that occurs without gate clock correction. Simultaneous gate clocks were used to examine the transient analysis. The clock circuit is given in figure 13.

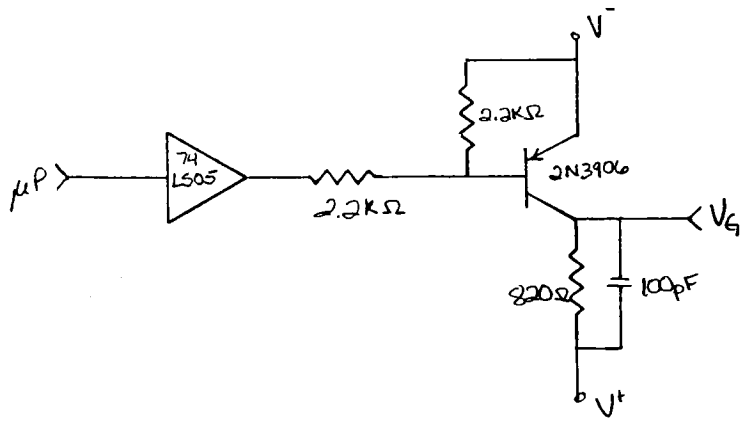


Figure 13. Asymmetrical Clock Circuit

The clocks were generated by microprocessor to circumvent inverter delays, insuring that the switching occurred simultaneously. The logic levels were buffered to drive levels and filtered for a quick rise and a slow fall. For this test, the source, substrate, and n-well were held at ground. Figure 14 shows the drain / capacitor node voltage, as measured with a Tektronix P6056 1 pF, 500 Ω, 300 MHz probe, and the p-channel clock. The n-channel clock is shown in figure 15. The transmission gate turn-off characteristics are pictured for an abrupt p-channel gate clock and a slow n-channel gate clock. The drain voltage increases with the transient from the p-channel device, and then falls with the arrival of the delayed n-channel transient. The transient waveforms were repeatable in all aspects but magnitude. This is likely the result of the previous voltage held on the capacitor and the indeterminate amount of time allowed for discharge. These waveforms were investigated in the simulations described later.

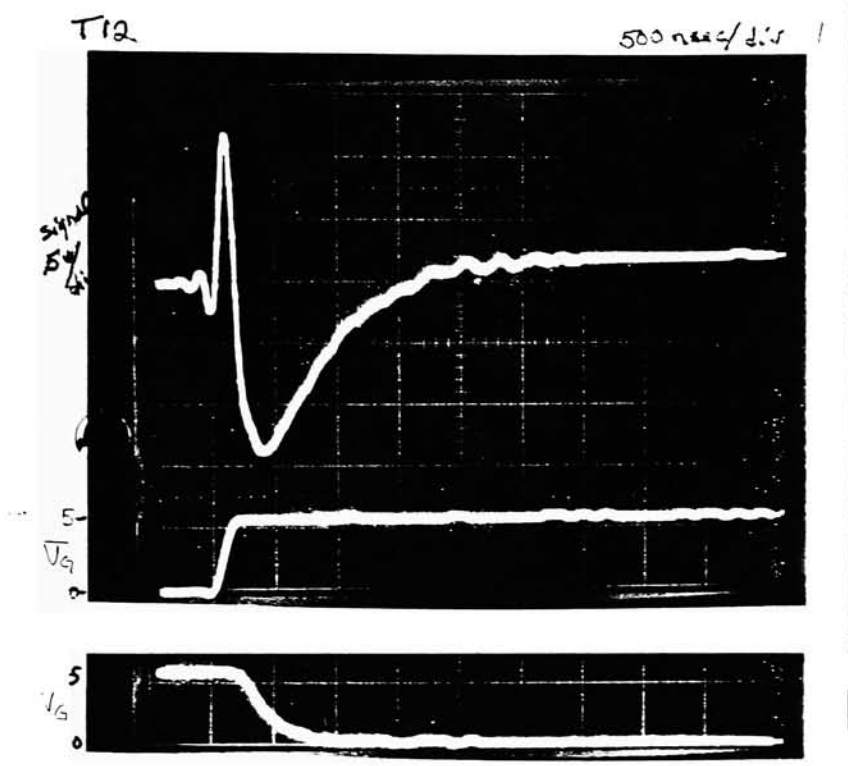


Figure 14 and 15. Drain Voltage and Gate Clocks

TRANSISTOR EVALUATION

Seven geometries of transistors were evaluated. Three were of interest because of their modified geometries and the remainder were used to characterize the Kodak CMOS process. All of these devices were tested using a Hewlett-Packard 4145 Semiconductor Parameter Analyzer. Three standard tests were performed on every transistor: I-V curves, transconductance curves, and threshold voltage curves. An explanation of the test procedure precedes the discussion on the several devices.

I-V TEST

This test verifies the presence of normal transistor behavior. It also determines the channel length modulation parameter, λ. A typical curve is shown in figure 16 and additional data are located in Appendix B. This test is performed by sweeping the drain voltage for various gate voltages. The substrate and source are held at ground potential. The n-well is biased to the highest voltage used, maintaining the reverse bias with the substrate. In the linear region, the drain current I_D is related to the gate-to-source and drain voltages by

$$I_D = \beta(V_{GS} - V_T)V_{DS} \qquad (4a)$$

where

$$\beta = \mu\varepsilon_{ox}W \,/\, 2t_{ox}L(1 + \lambda V_{DS}) \qquad (2b)$$

The threshold voltage, V_T, can be measured with this test. It is typically defined as the voltage at which a predetermined amount of drain current flows. However, the choice of current level is rather arbitrary, and as a result, other measurement techniques are more commonly applied.

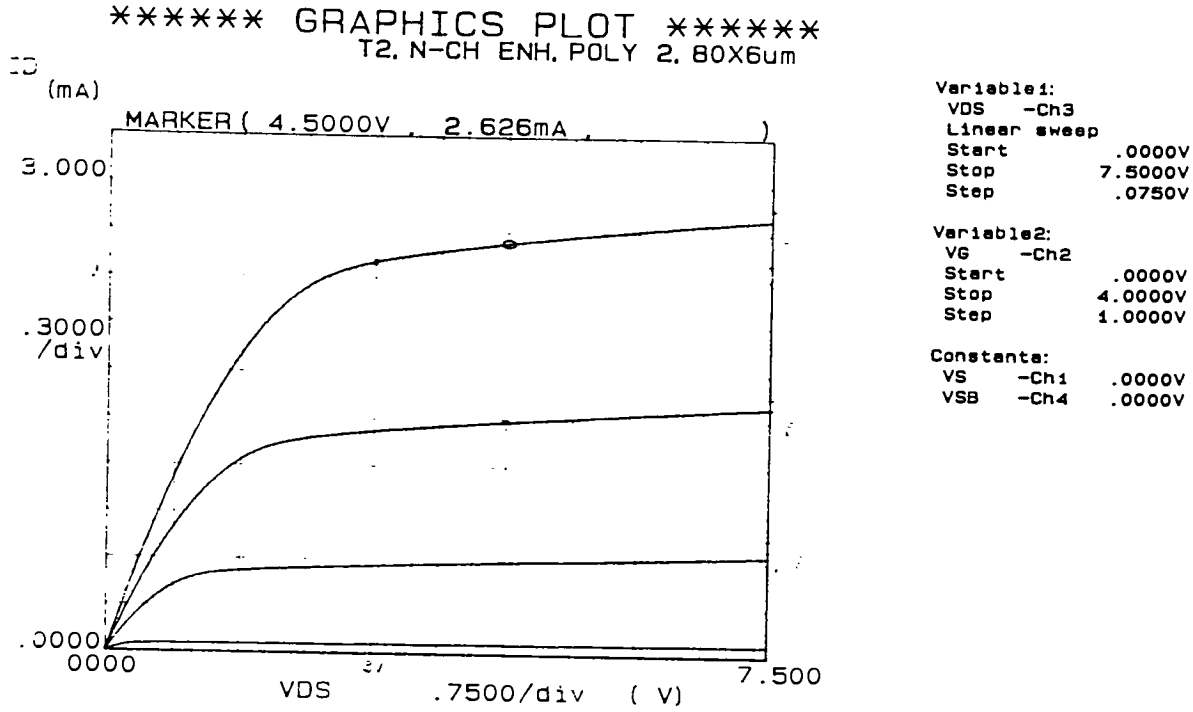


Figure 16. Typical I-V Curve

g_M TEST

The transconductance is the device's ability to vary I_D with varying V_G and constant V_{DS}.

$$g_M = dI_{DS} / dV_{GS} \quad | \ V_{DS} \text{ constant} \tag{5}$$

The test reflects changes in mobility with applied fields and provides a precise measurement of the threshold voltage. The transconductance test is performed by sweeping the gate voltage for various drain-to-source voltages. Again, the substrate and source are held at ground potential and the n-well at a positive potential. A typical curve is shown in figure 17 and additional data are located in Appendix B. The threshold voltage is measured

by extrapolating along the rising edge of the family of transconductance curves down to the gate voltage axis.

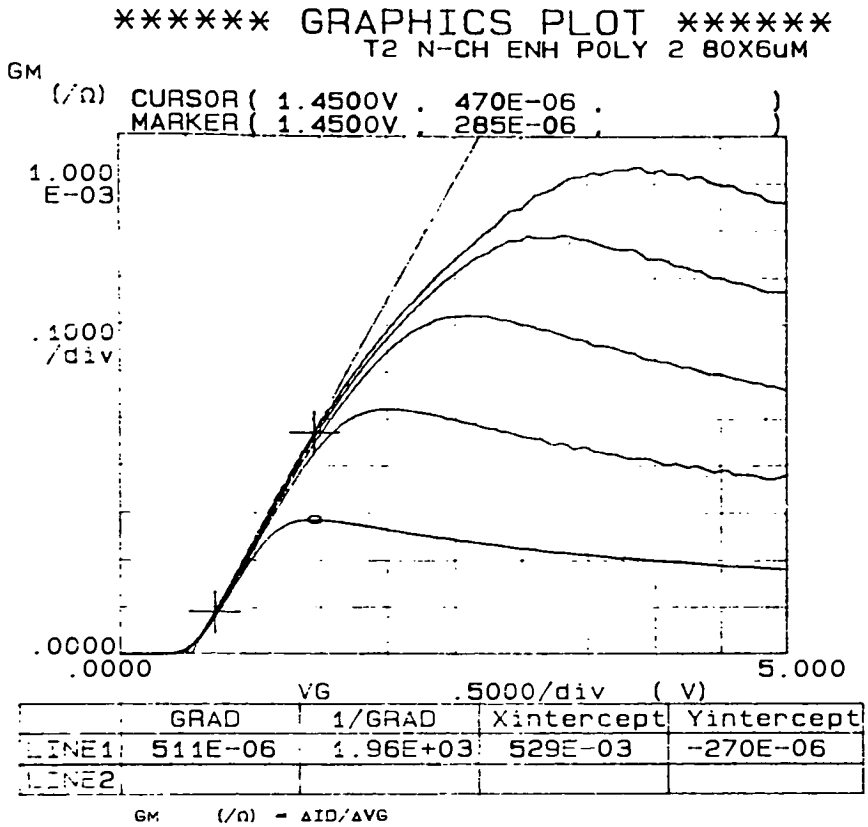
V_T, Gamma

As previously discussed the threshold voltage, V_T, and the body effect factor, γ, are important for accurate modeling of transmission gates. Gamma accounts for the shift in threshold voltage with substrate bias. This test is performed by sweeping the gate and drain voltages together for various substrate or n-well biases. Sweeping the gate and drain voltages together keeps the device biased in the saturation region. The gate voltage is plotted against the square root of the drain current since for saturation,

$$\sqrt{I_{Dsat}} = \sqrt{\beta}\ (V_{GS} - V_T) \qquad (6a)$$

Extrapolating the curves back to the V_G axis gives the threshold voltage, V_T, for a particular substrate bias, V_{SB}. Measurement of V_T for a number of substrate biases on each device allows accurate calculation of the desired parameters even with uncertainty in substrate doping, N_{sub}.

A typical curve is shown in figure 18 and additional data are contained in Appendix B.

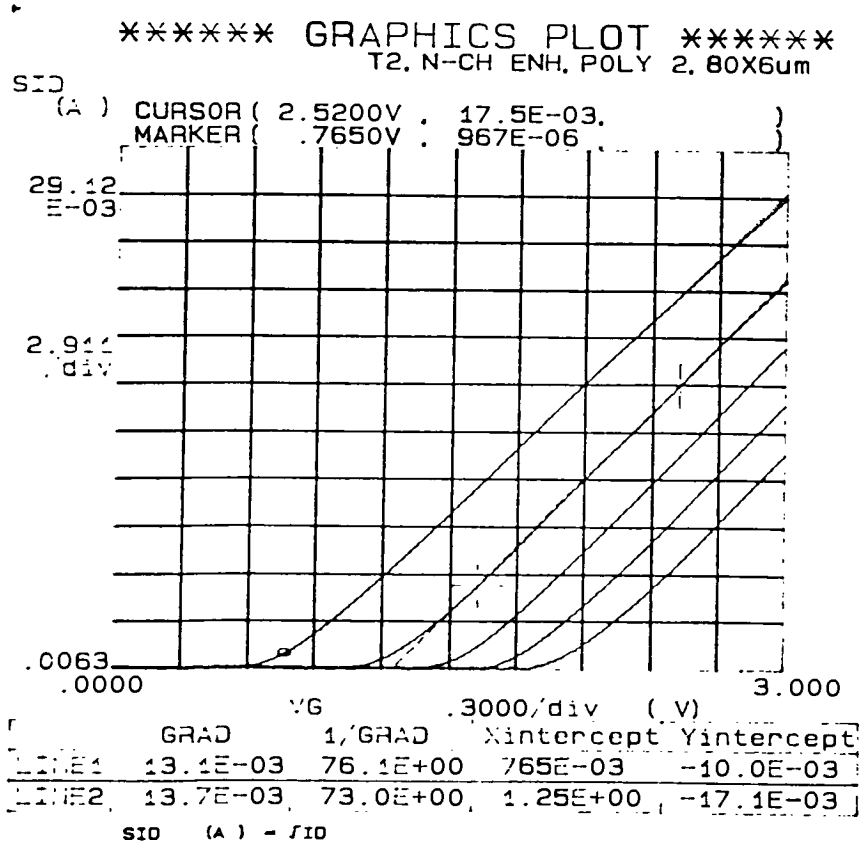


Variable1:
VG -Ch2
Linear sweep
Start .0000V
Stop 5.0000V
Step .0500V

Variable2:
VD -Ch3
Start .5000V
Stop 2.5000V
Step .5000V

Constants:
VS -Ch1 .0000V
VSB -Ch4 .0000V

Figure 17. Typical g_M curve



Variable1:
VG -Ch2
Linear sweep
Start .0000V
Stop 3.0000V
Step .0300V

Variable2:
VSB -Ch4
Start .0000V
Stop -4.0000V
Step -1.0000V

Constants:
VS -Ch1 .0000V

Figure 18. Typical V_T, γ curve

MODIFIED GATE AND CHANNEL TRANSISTORS

A test structure containing modified n-channel transistors was examined. Three devices in this test structure were of interest. An unmodified device served as a reference for a flared buried channel device and a segmented drain device. The geometries of the devices are important because both modifications could reduce the channel-to-drain contact area and the gating feedthrough charge, which is dependent on channel area and symmetry. The three devices were of the same length and width, two microns.

The flared buried channel device was fabricated with a nonrectangular buried channel mask. As illustrated in figure 19, the channel implant narrows significantly at the drain connection.

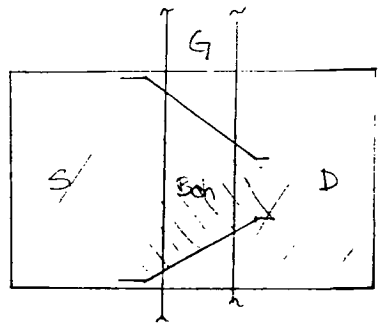


Figure 19. Flared Buried Channel FET

The other device, the segmented drain FET, was laid out with a digitated rather than a uniform edge along the channel boundary. The structure is shown in figure 20. The device design provided for various drain-to-channel separations. The means provided for the variation was intentional mask misalignment during fabrication.

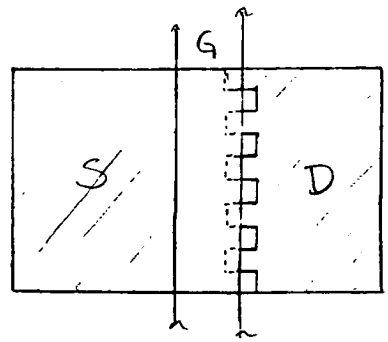


Figure 20. Segmented Drain FET

The tests previously described were performed on thirty of these structures. Typical curves from the tests are contained in Appendix A. The segmented drain devices mimicked the performance of the normal devices, with slightly reduced currents. Upon close examination, no sign of the segmented drain was apparent. A photomicrograph of the device is shown in figure 21. It is reasonable to expect that the slight variation from normal is due to the segmentation under the drain. Unfortunately, processing data were not available on any of these devices, precluding complete characterization.

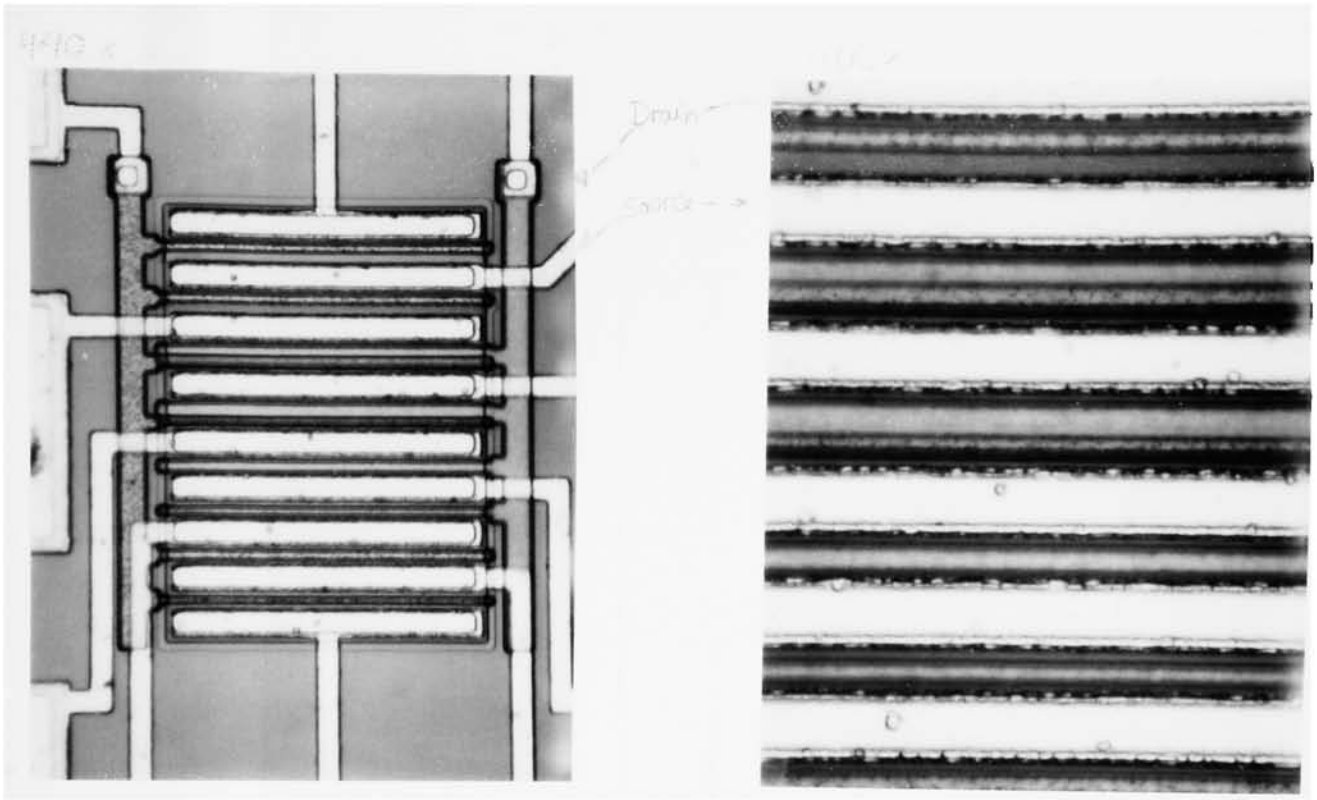


Figure 21. Micrograph of Segmented Drain Device

The data from the flared buried channel devices are more unusual. The I-V curves do not exhibit the expected behavior. They appear to be resistive in nature, with a slight variation due to body effect. Lack of process data on these devices precludes an explanation of this behavior.

CHARACTERIZATION MEASUREMENTS

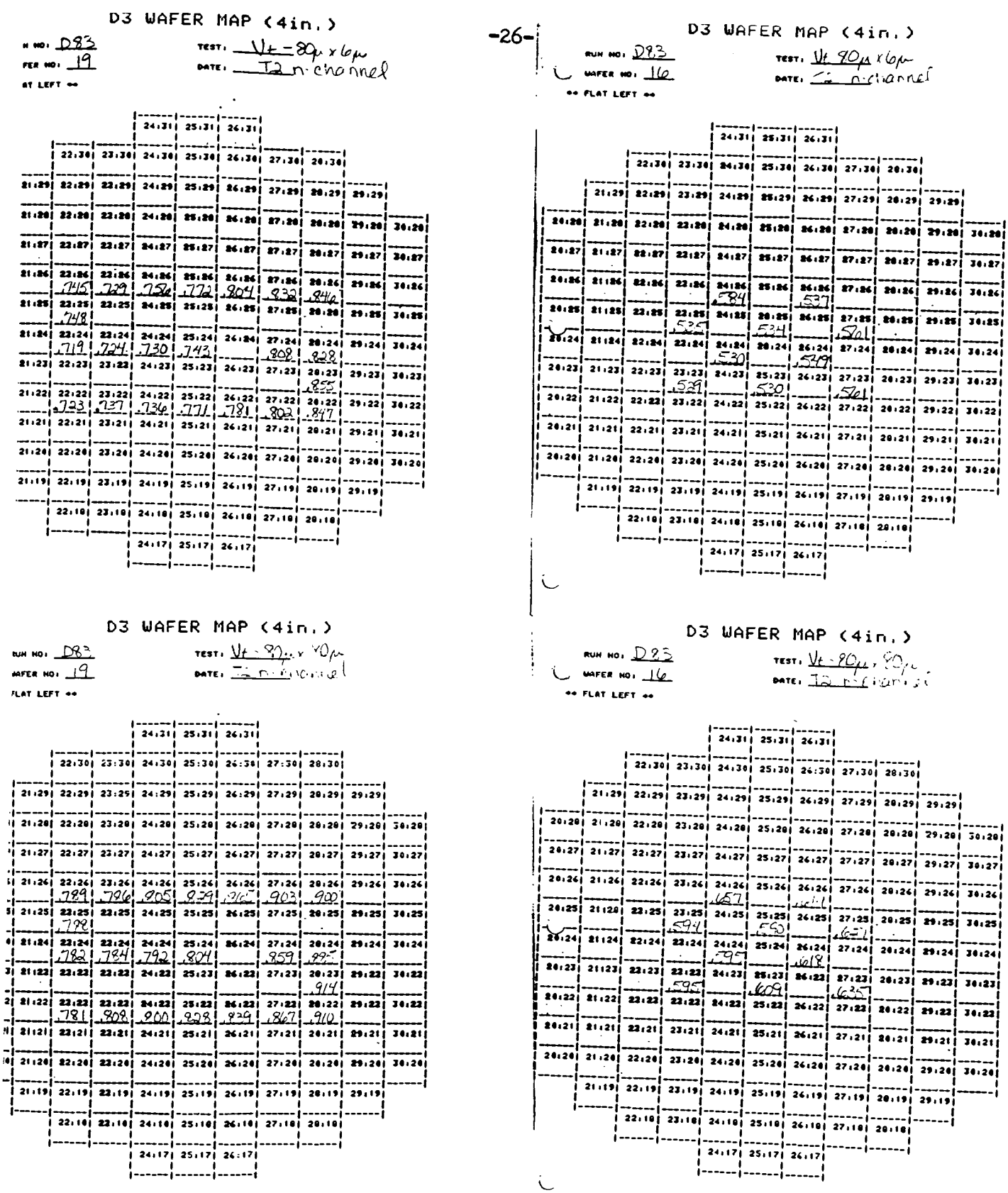
A group of 84 standard transistors consisting of channel lengths of 6u and 80u for both n- and p-channel devices were examined. The n-channel devices are identified as T26 and T280 (test structure 2)

and the p-channel devices are similarly identified as T46 and T480. The previously described tests were also performed on these devices. Data were taken on two wafers. The first test group, wafer D8319, had nonfunctional p-channel devices, therefore only n-channel data are presented. The second data set, wafer D8316, contains both n- and p-channel measurements. Data from these sets are presented and summarized in Appendix B. The variance in the data indicates that there is no significance in taking 25 data points rather than 10 data points. A trend of possible interest was observed in the threshold voltage data. The device threshold voltage and its location on the wafer can be seen in figure 22. The voltages increase with increasing row and column. In layouts which require precision device matching, this information may be useful.

Modeling parameters for use with SPICE were derived from a combination of measurements and data from both the process report and process design specifications.

Data from the process design specification were low voltage mobility, μ_0, junction depth, x_j, lateral diffusion, L_D, and type of gate, t_{pg}; if polysilicon gates are used, dopant polarity must be noted.

Important data from the device run process sheet were gate oxide thickness, t_{ox}, drain and source sheet resistance, R_{sh}, and nominal wafer dopant concentration, N_{sub}.



In each case, V_T increased with column and row number.

Figure 22. Die Position vs. V_T

From the I-V curves, the channel modulation parameter λ is determined by evaluating the slope in the saturation region of operation. From the derivative of equation (2) the slope can be defined as

$$dI_D/dV_{DS} = \frac{d\{ (\mu\varepsilon_{ox}W / 2t_{ox}L)(V_{GS} - V_T)^2\}}{dV_{DS} \quad (1 + \lambda V_{DS})}$$

$$= \frac{\lambda (\mu\varepsilon_{ox}W / 2t_{ox}L)(V_{GS} - V_T)^2}{(1 + \lambda V_{DS})^2}$$

$$= \lambda I_D / (1- \lambda V_{DS}) \qquad (8)$$

Using curves of I_D and V_{DS}, λ can be determined algebraically.

Measurement of V_T for a number of substrate biases, V_{SB}, on each device allows accurate calculation of some desired parameters even with uncertainty in substrate doping, N_{sub}. V_T can be calculated for any substrate bias from

$$V_T = V_{T0} - \gamma\{ \sqrt{(V_{SB} + 2\phi_f)} - \sqrt{(2\phi_f)}\} \qquad (9)$$

In the first iteration, ϕ_f was calculated from

$$\phi_f = KT/q \ln(N_{sub}/n_i) \qquad (10)$$

with the value of N_{sub} taken as the median from the process specifications. Then by performing a linear regression on the measured V_{SB} and V_T data pairs with the form

$$y = b \quad - m\{ \quad x \quad \} \tag{11}$$

where

$$V_T = V_{T0} - \gamma\{ \sqrt{(V_{SB} + 2\phi_f)} - \sqrt{(2\phi_f)}\} \tag{9}$$

values for V_{T0} and γ result. Next, γ was used to determine N_{sub} from

$$\gamma = \sqrt{(2N_{sub}q\varepsilon_{Si})} \; / \; C'_{ox} \tag{12}$$

The values for N_{sub} resulting from the measurements on 80μ and 6μ devices were compared. Since the devices were neighbors on the wafer, it is reasonable to assume that N_{sub} was the same for both. An average value for N_{sub} was then used to recalculate ϕ_f. The procedure was iterated until N_{sub} settled to a stable value. This procedure was performed on a personal computer using a readily available equation-solving software package. The worksheets and results are contained in Appendix C. Other SPICE variables required straight-forward calculation such as N_{ss}, C_{jsw}, C_j, C_{GSO}, C_{GDO}, and P_B.

RESULTS

CMOS PROCESS PARAMETERS

From the test transistor measurements and process sheet information, a SPICE parameter model for transistors in the Eastman Kodak CMOS process was derived. These parameters, given in table 4, for the n- and p-channel FET's, are identical for the 6u and 80u devices except for λ, the channel length modulation factor. To verify the parameters' fit, the I-V curve tests were simulated, figures 23-26. The SPICE simulation curves, in asterisks, are overlaid on the device data collected with the Hewlett Packard 4145 Semiconductor Parameter Analyzer. The agreement between the measured and simulated data is very good and is detailed in table 3. To fit the p-channel transistor curves, the n-well bias was adjusted to 4.7 volts rather than 5 volts as in the actual device tests. The n-well bias affects the spacing between the I-V curves, the current at a given V_{GS} and V_D. This adjustment indicates that the resistances in the contact and through the tub diffusion are significant.

Device	V_{DS}	V_G = 4v	3v	2v
T280	4.5v	.6%	2.1%	1.3%
	7.5v	.3%	1.6%	.8%
T26	4.5v	1.4%	11.8%	16.4%
	7.5v	1.6%	8.5%	18.3%
T480	4.5v	.7%	1.6%	1.3%
	7.5	1.2%	1.1%	.8%
T46	4.5v	.1%	5.3%	11.4%
	7.5v	2.8%	2.3%	9.3%

Table 3. Percent Difference in Simulated and Measured I-V Curves

NAME	T2		T4	
TYPE	NMOS		PMOS	
LENGTH	6um	80um	6um	80um
LEVEL	2.000	2.000	2.000	2.000
TPG	1.000	1.000	-1.000	-1.000
TOX	7.11D-08	7.11D-08	7.11D-08	7.11D-08
NSUB	4.01D+14	4.01D+14	3.70D+16	3.70D+16
XJ	5.00D-07	5.00D-07	8.00D-07	8.00D-07
LD	2.00D-07	2.00D-07	6.00D-07	6.00D-07
UO	610.000	610.000	178.000	178.000
KP	2.96D-05	2.96D-05	8.65D-06	8.65D-06
VTO	0.530	0.604	-1.070	-1.009
GAMMA	0.223	0.251	0.665	0.774
PHI	0.529	0.529	0.763	0.763
LAMBDA	1.75D-02	1.55D-03	2.75D-02	1.55D-03
PB	0.871	0.871	0.719	0.719
RSH	48.920	48.920	285.600	285.600
CGSO	2.91D-10	2.91D-10	4.85D-10	4.85D-10
CGDO	2.91D-10	2.91D-10	4.85D-10	4.85D-10
CJ	1.77D-04	1.77D-04	9.58D-06	9.58D-06
CJSW	8.85D-11	8.85D-11	9.58D-12	9.58D-12
MJ	0.500	0.500	0.500	0.500
MJSW	0.300	0.300	0.300	0.300
NSS	4.76D+11	4.98D+11	1.29D+11	1.48D+11

Table 4. SPICE 2G.5 Parameters for EK CMOS Process

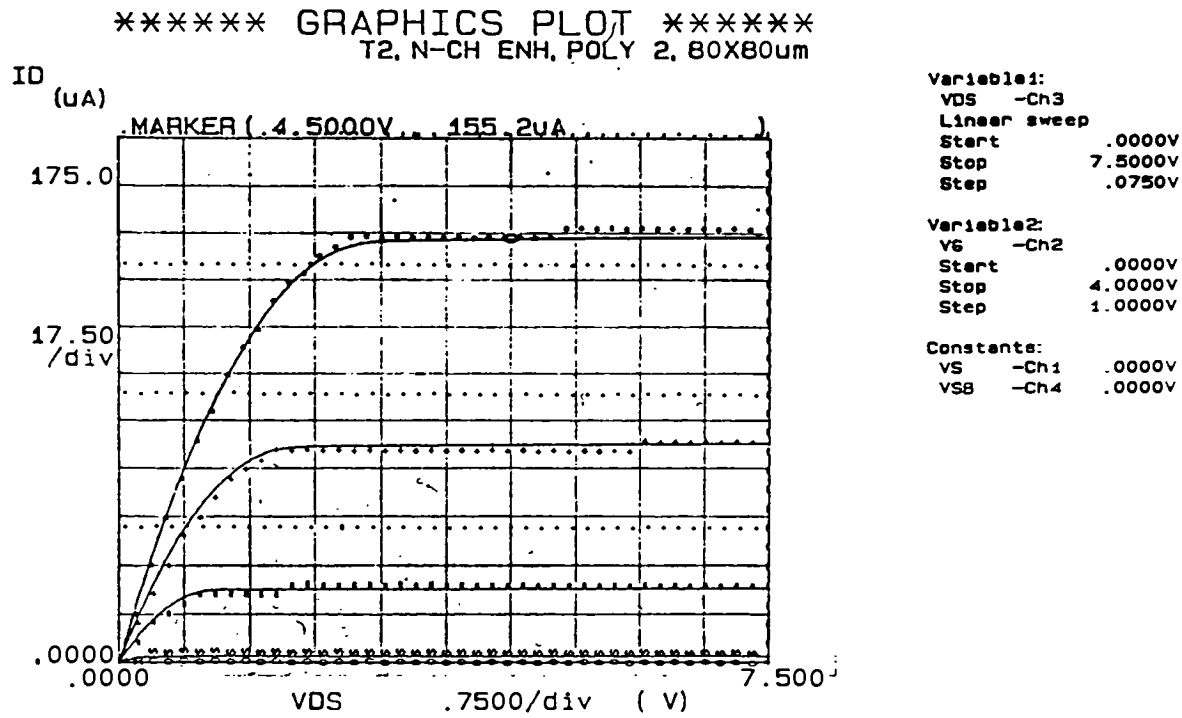


Figure 23. I-V Curve: Model and Data for T2 80um

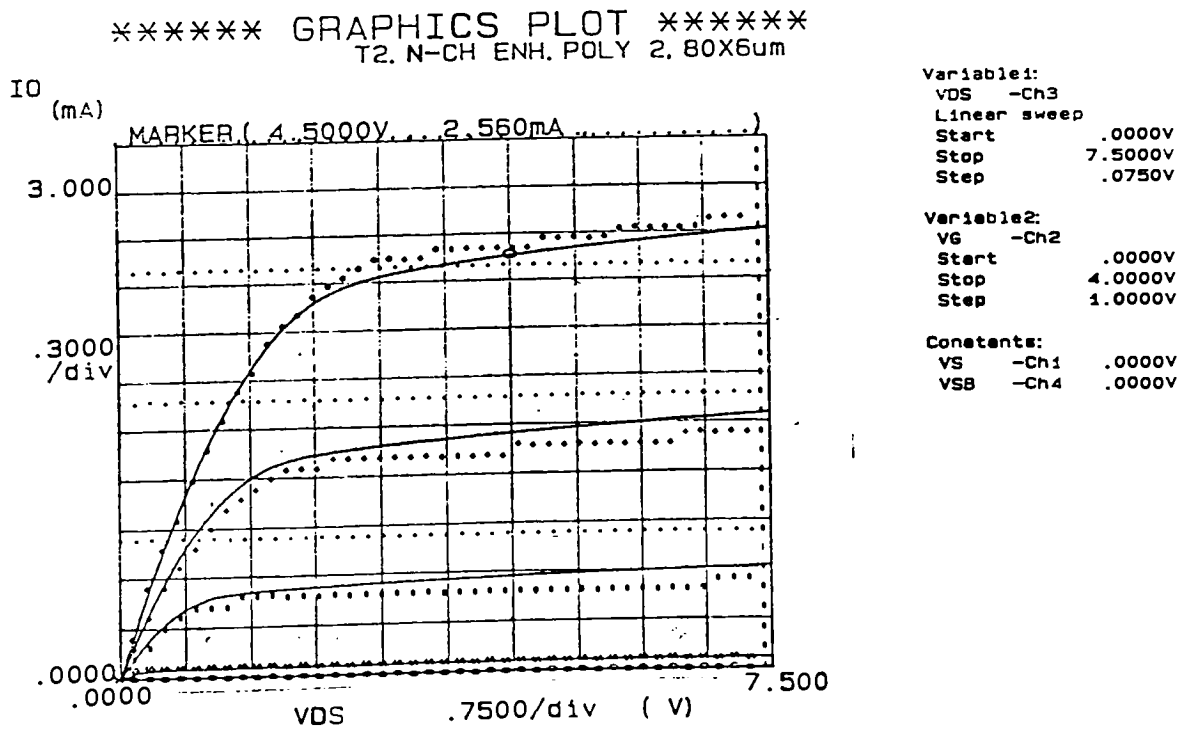


Figure 24. I-V Curve: Model and Data for T2 6um

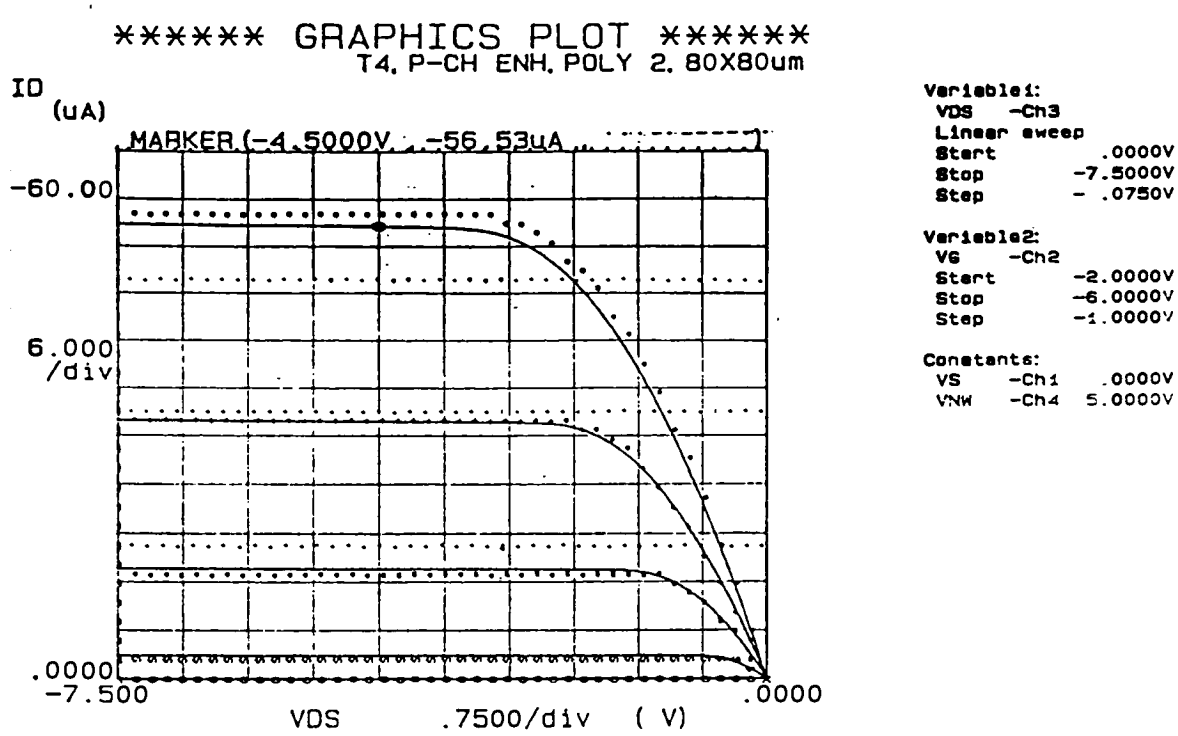


Figure 25. I-V Curve: Model and Data for T4 80um

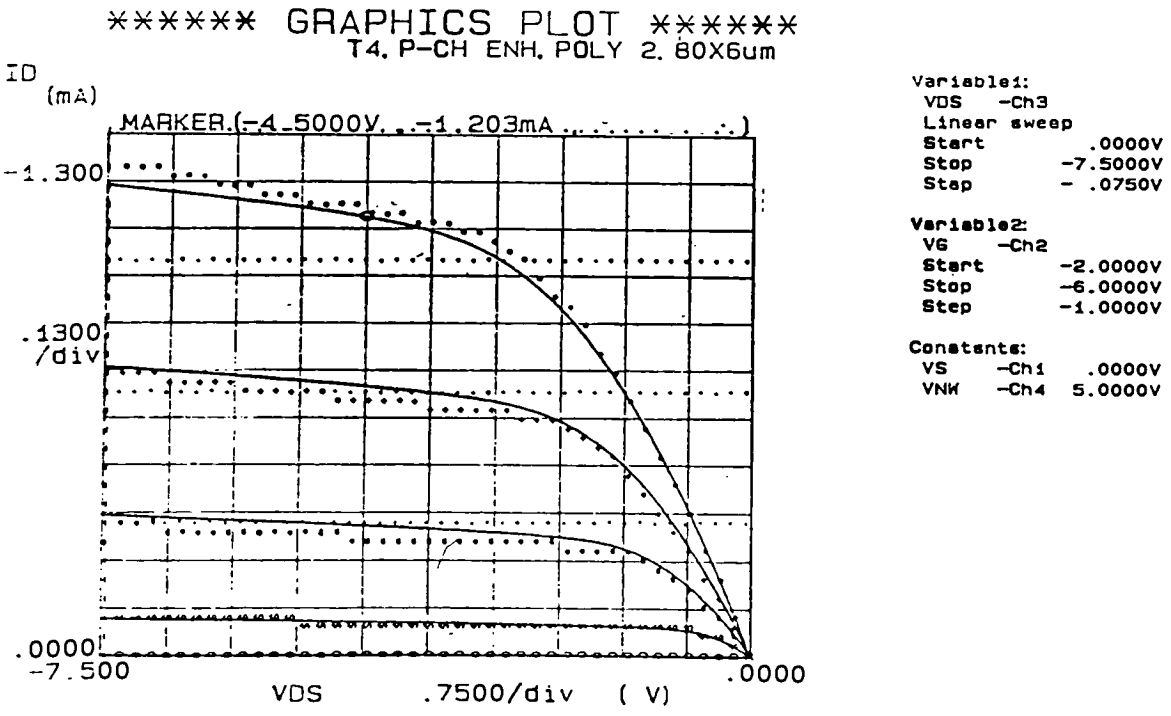


Figure 26. I-V Curve: Model and Data for T4 80um

TRANSMISSION GATE MODEL AND TIMING REQUIREMENTS

To evaluate the feedthrough transient, a standard transmission gate was simulated. The circuit model is shown in figure 27.

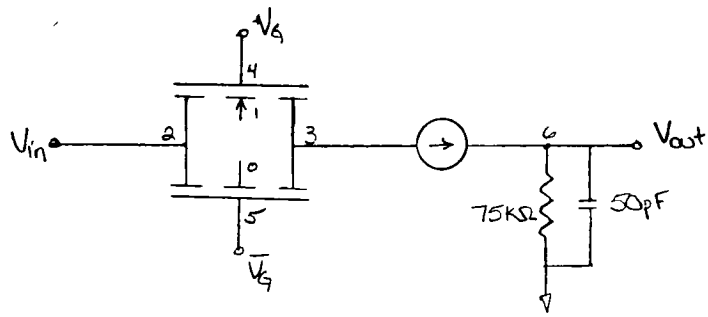


Figure 27. Transmission Gate SPICE Model

A series of simulations was run with this model. The figures described here are the result of simulations which are documented in Appendix D.

First, with the p-channel device held off, V_G = 1v, a step impulse was given to the n-channel gate, V_G = -1v to 5v. The feedthrough at the drain node and the clock pulse are plotted in figure 28. The drain voltage goes positive because electrons are pulled into the channel during device turn-on. Next, the n-channel device was held off, V_G = 0v, and the p-channel gate was given a step impulse, V_G = 1v to -6.5v. Again, the drain voltage and the clock pulse are plotted in figure 29. In this configuration, the node voltage goes negative because the positive holes are pulled into the channel.

In figure 30, both transistors are initially off, V_{GP} = 1v, V_{GN} =

-1v, then enabled sequentially, V_{GP} = -6.5v. V_{GN} = 5v. The magnitude of the negative transient is reduced by the tail of the positive transient, as seen earlier in the transmission gate test structure evaluation. The ideal operation of this structure should occur when the gate clocks are adjusted so that the two transients cancel each other. Figure 31 shows the effect when both clocks are enabled simultaneously. The time scale in this plot has been reduced to show the early departure of the electrons, creating a positive transient. As was discussed earlier, it is important to compensate for the lower mobility of holes in the p-channel device by turning it on and off before the n-channel device.

Reducing the slope of the n-channel clock to slow the rate of carrier migration aids in cancelling the transients, as can be seen in figure 32. It should be noted that the linear rise of the clocks modelled by SPICE are different from the R-C filters commonly used.

Figures 33-35 demonstrate both the effect and the high sensitivity of the gate clock timing. In figure 33 the n-channel clock lags by .03 nanosecond, in figure 34 the lag is .04 nanosecond, and in figure 35 the lag is .05 nanosecond. A reduction in the transient magnitude of 30 to 50 dB can be realized, but the clock placement is too sensitive for practical use. The amount of reduction will also be affected by fluctuations in gate and signal voltages, and by temperature.

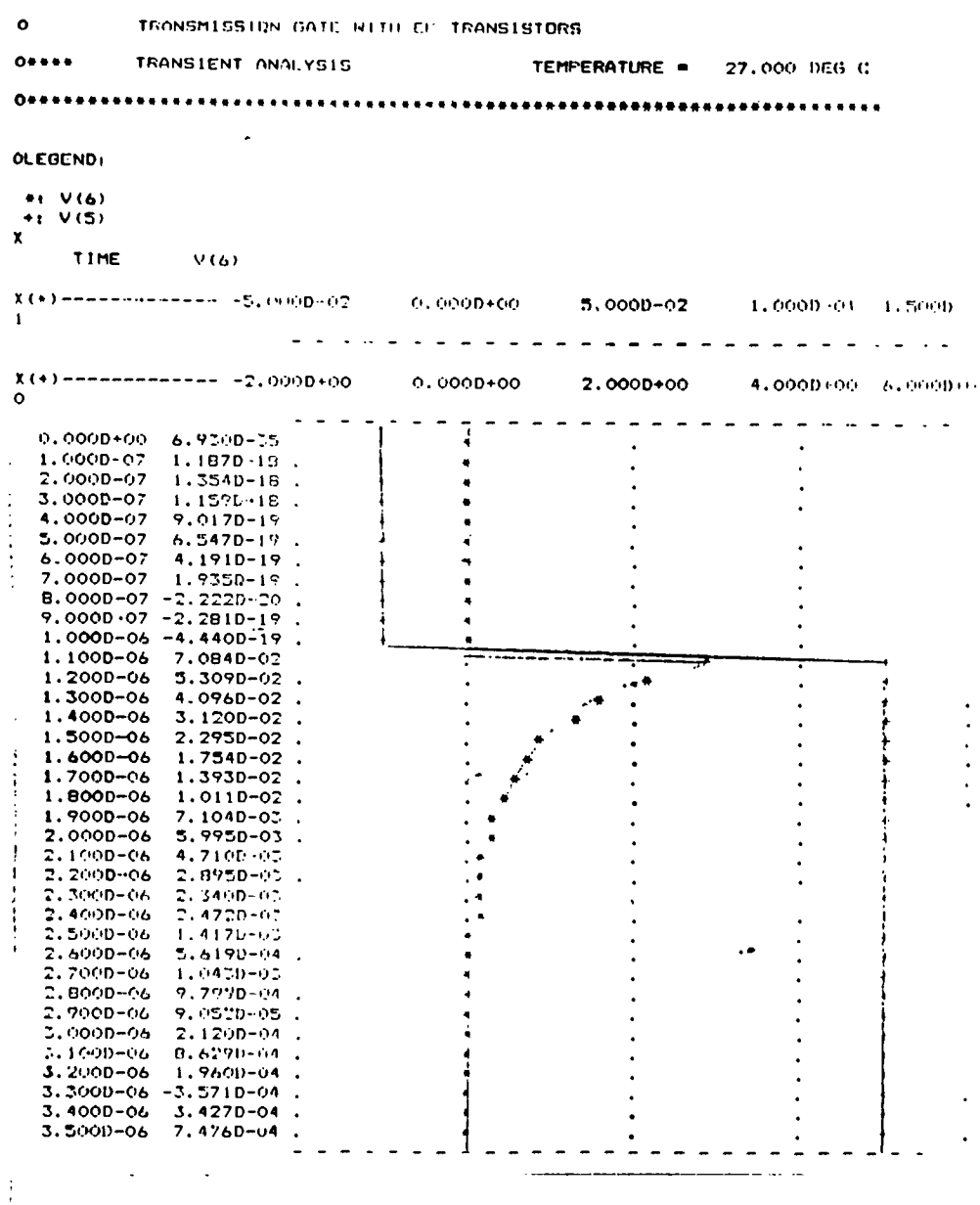


Figure 28. Model of N-Channel Transient

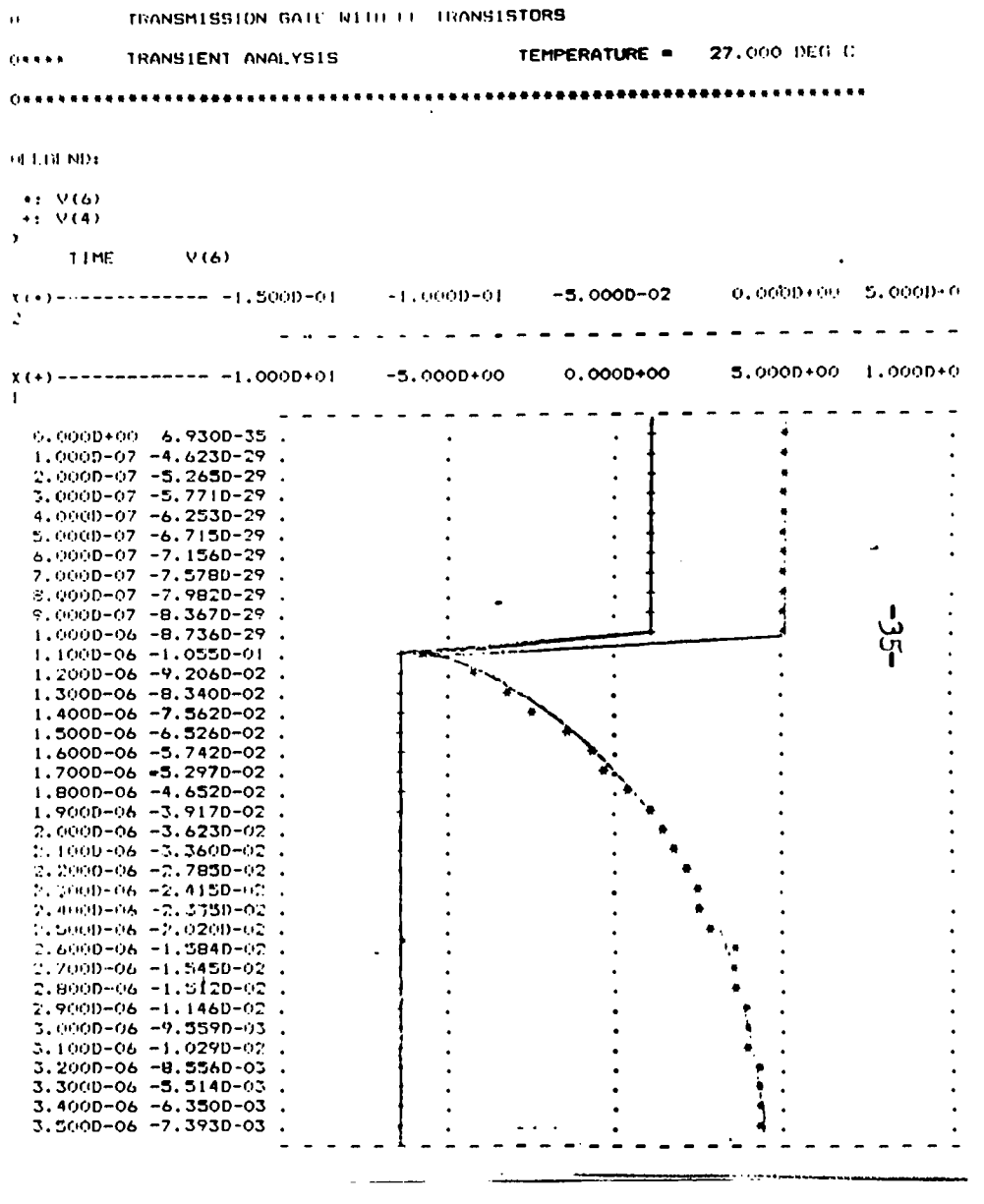


Figure 29. Model of P-Channel Transient

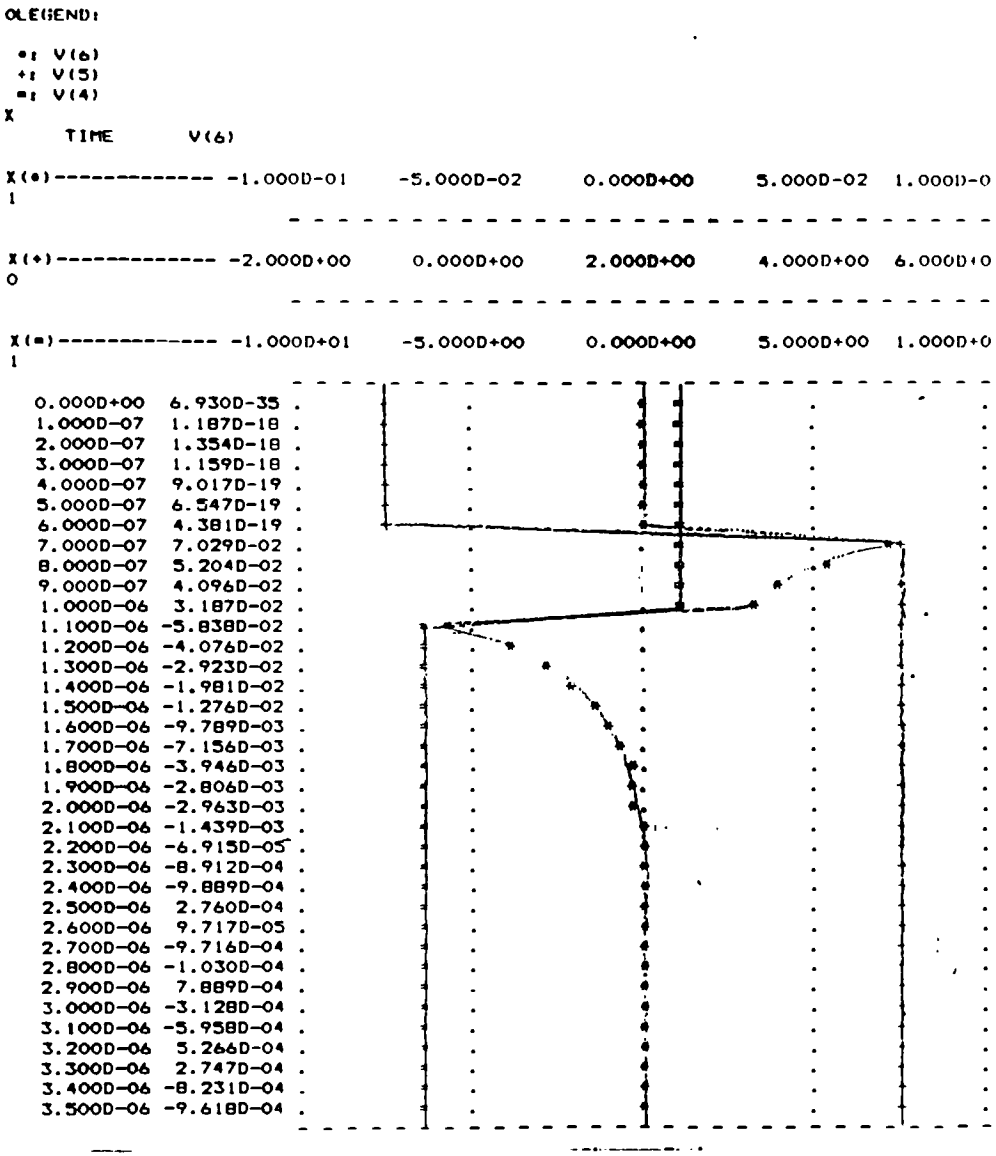


Figure 30. Model with Misaligned Gate Clocks

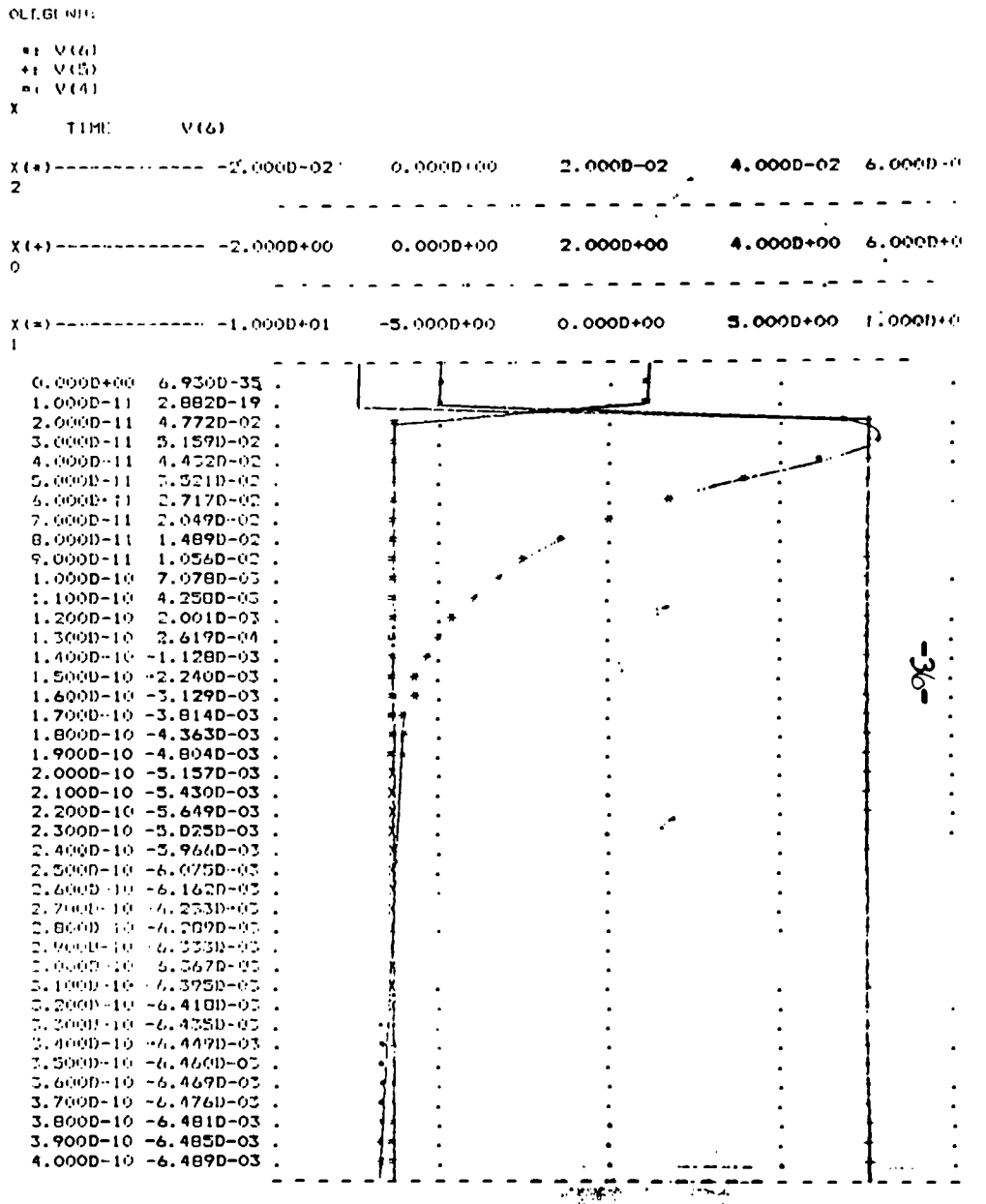


Figure 31. Model with Aligned Gate Clocks

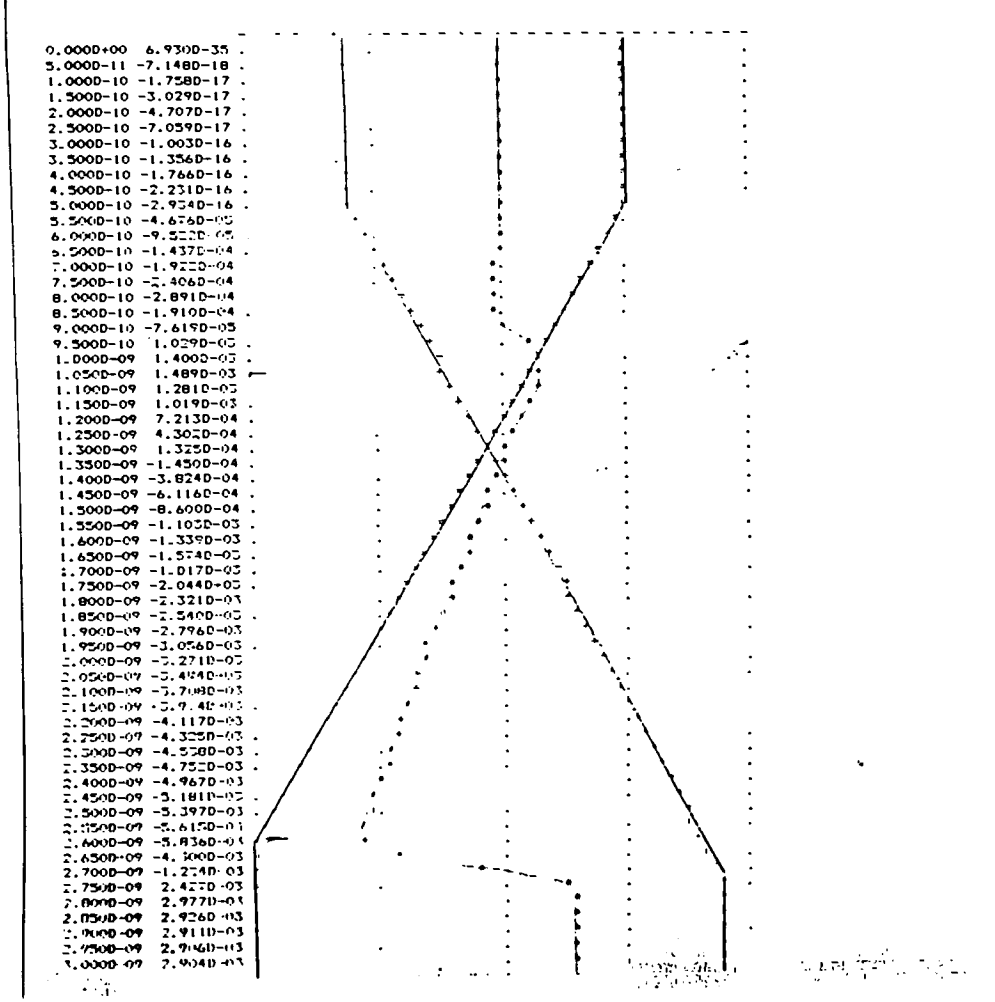


Figure 32. Model with Retarded N-Channel Clock Slope

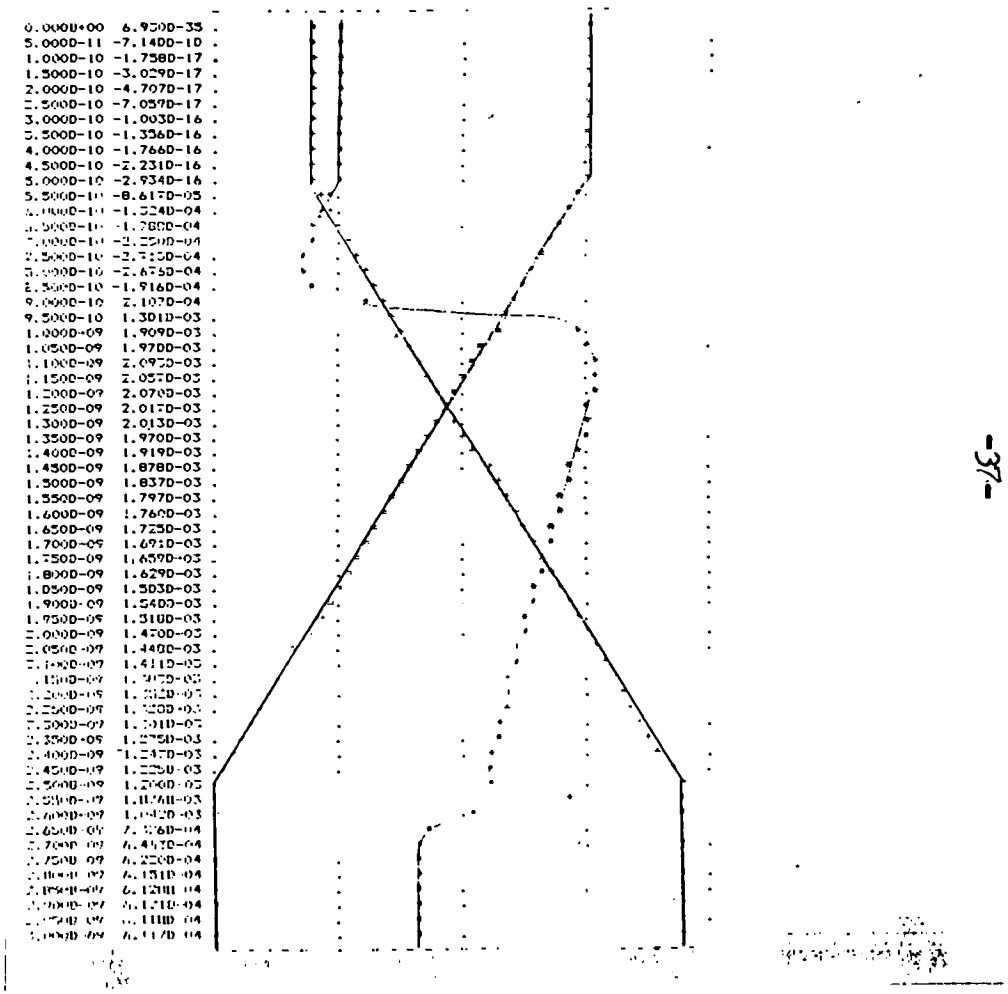


Figure 33. Model with .03 nsec N-Channel Clock Lag

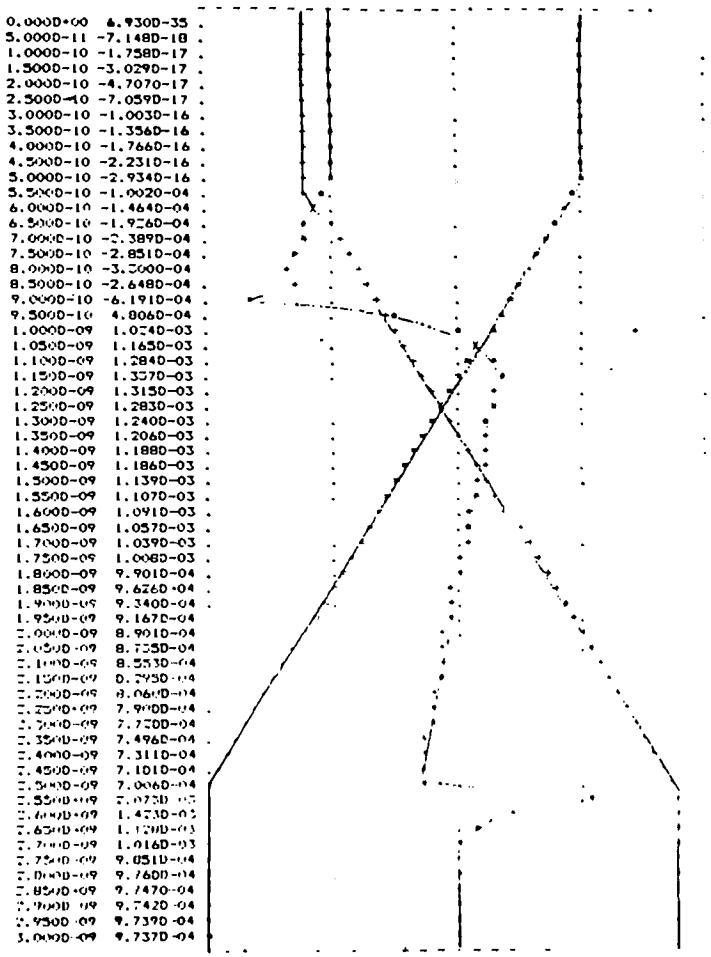


Figure 34. Model with .04 nsec N-Channel Clock Lag

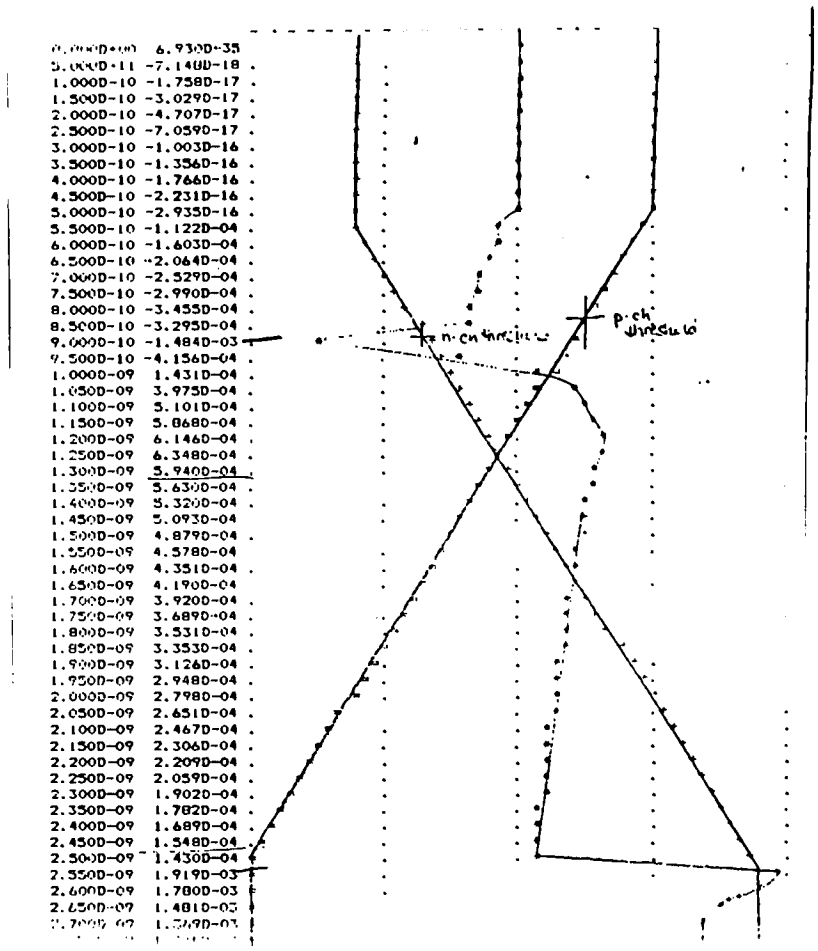


Figure 35. Model with .05 nsec N-Channel Clock Lag

PROPOSED STRUCTURE FOR IMPROVED PERFORMANCE

The transmission gate structure has evolved from a single FET through an FET with a dummy channel which contributed charge of opposite polarity for cancellation of feedthrough transients. This progressed to two functional FET's removing the limitation on input signal swing, while offering the potential for feedthrough transient cancellation. The main problem now is to make this cancellation practical and effective. It is impractical to add enough control circuitry to make the necessary gate clock voltage and timing adjustments that track temperature and signal level.

An alternative approach to the problem is to put aside the notion of balancing the channel charge transients at the output node and never let them go there. A possible technique is to conserve the channel charge by transferring it to an adjacent storage capacitor structure. By providing a favorable path between the channel and this storage capacitor, the channel charge will not follow the path to the output node. Similar paths are already used to transfer photodiode or photocapacitor charge to output registers. A possible configuration is shown in figure 36.

The clocking for this structure could be very much like that for other charge coupled devices (CCD's). The storage gate should be enabled followed by an enable on a transfer gate while the switching gate begins its fall. With this technique, the amount of charge in the transient can be controlled for many sizes of devices.

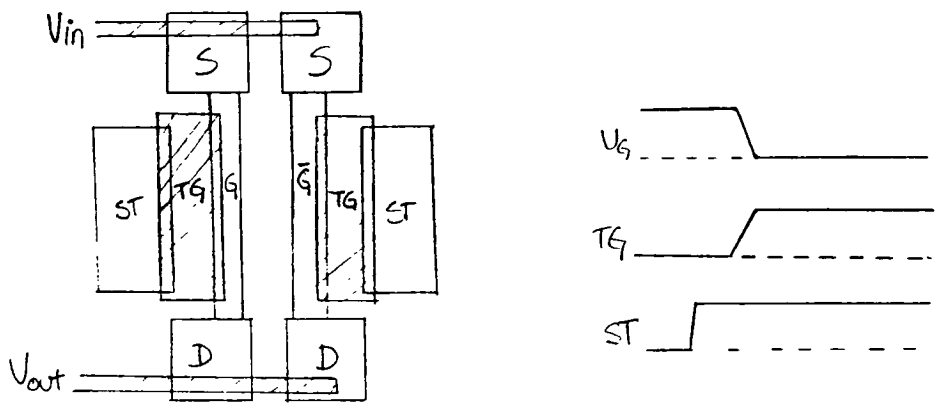


Figure 36. New Transmission Gate Structure

CONCLUSIONS

The problem of gating feedthrough in CMOS transmission gates has been reviewed. A variety of structures have been tested and an accurate model for the Eastman Kodak CMOS process has been developed. Using this model, I-V curves were simulated to test the goodness of fit between the model and data. The agreement is typically within 2% for saturated devices. Analysis of gate clock timing requirements indicates considerable sensitivity to relative device turn-on times. Since this is difficult to control in practical application, an alternate technique which circumvents this sensitivity problem is recommended. It is also recommended that further study be given to the modified channel transistors. These devices may provide additional benefit, but there is not enough data available at this time to base a conclusion.

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APPENDIX A

MODIFIED GATE AND CHANNEL TRANSISTOR DATA

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Normal Devices 2u

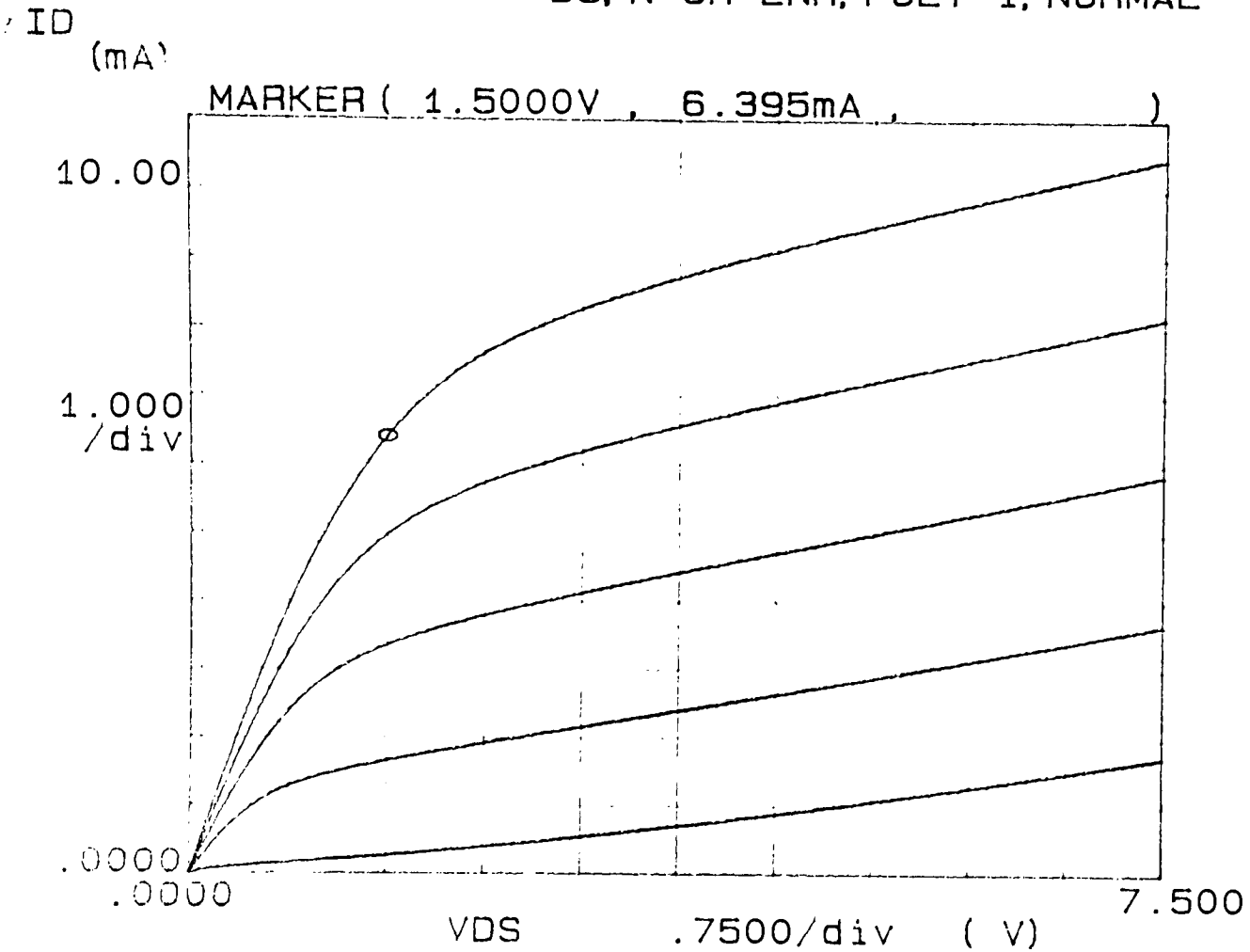
Wafer Location	W @1.5v mil	Vto	gm gm(max1) m/Ohms	Vt Vsub=0	Vt Vsub=-4	Body Effect Vs Vsub=-4
24 23	6.395	-0.717	0.978	0.725	0.891	
26 25	6.362	0.720	0.970	0.724		0.709
28 27	5.276	-0.821	0.943	0.678	0.867	
27 34	6.143	-0.636	0.928	0.781	0.969	
25 24	6.613	-0.765	1.010	0.707	0.870	
24 31	6.178	0.664	0.925	0.757	0.921	
26 35	6.110	-0.606	0.923	0.827	0.905	
28 35	6.552	-0.873	0.998	0.664	0.824	
27 36	6.406	-0.831	0.970	0.713	0.891	
25 36	6.248	-0.640	0.917	0.764	0.945	
Avg	6.243	-0.726	0.957	0.734	0.892	0.709
Std	0.360	0.089	0.031	0.047	0.049	
Dev	5.8%	12.23	3.26	6.33	5.44	
Var	0.134	0.008	0.001	0.002	0.00?	

From regression analysis:

Gamma	Vto
0.051	0.734

****** GRAPHICS PLOT ******

D5, N-CH ENH, POLY 1, NORMAL



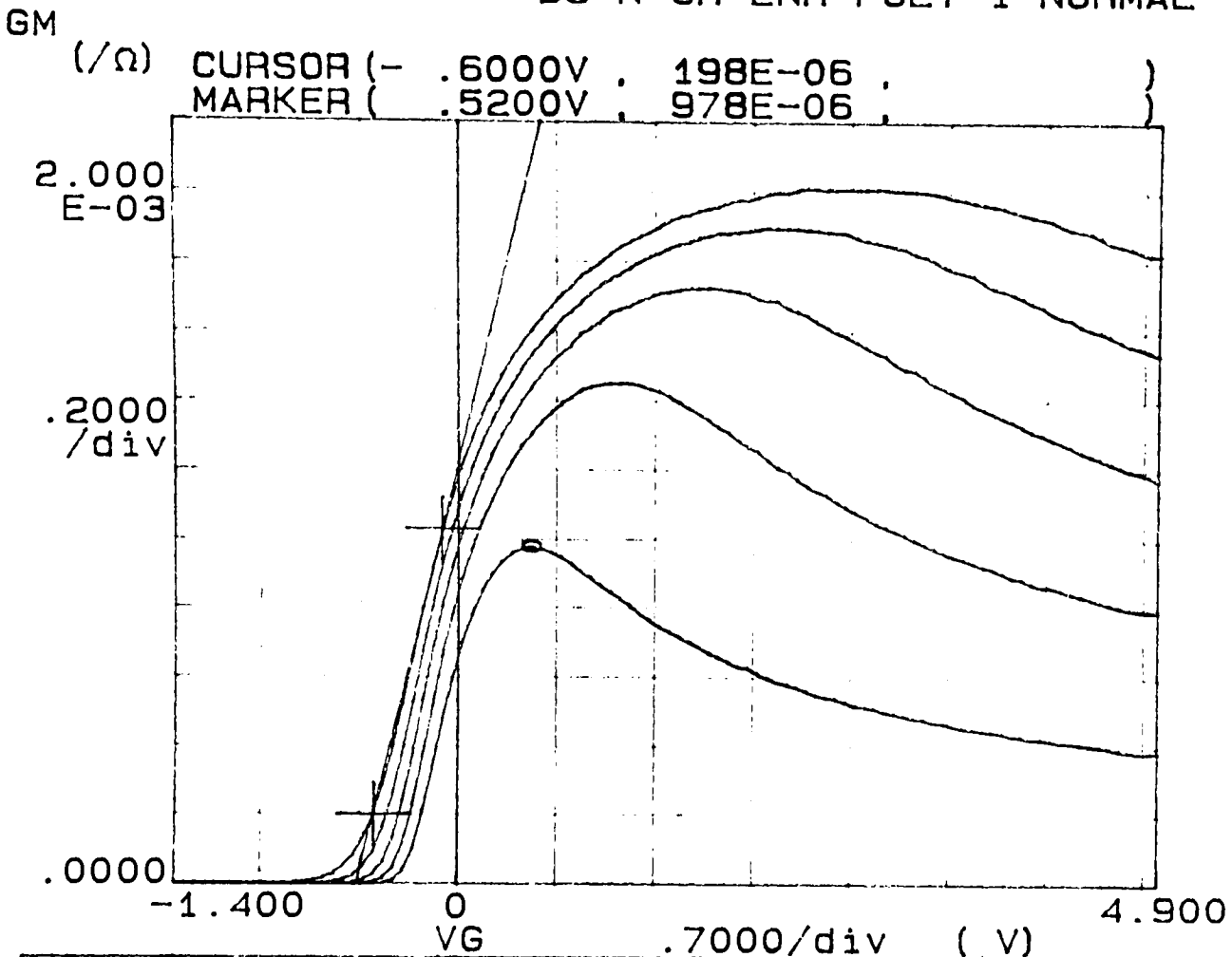
Variable1:
VDS -Ch3
Linear sweep
Start .0000V
Stop 7.5000V
Step .0750V

Variable2:
VG -Ch2
Start .0000V
Stop 4.0000V
Step 1.0000V

Constants:
VS -Ch1 .0000V
VSB -Ch4 .0000V

****** GRAPHICS PLOT ******

D5 N-CH ENH POLY 1 NORMAL



	GRAD	1/GRAD	Xintercept	Yintercept
LINE1	1.69E-03	591E+00	-717E-03	1.21E-03
LINE2				

GM (/Ω) = ΔID/ΔVG

Variable1:
VG -Ch2
Linear sweep
Start -2.0000V
Stop 5.0000V
Step .0700V

Variable2:
VD -Ch3
Start .5000V
Stop 2.5000V
Step .5000V

Constants:
VS -Ch1 .0000V
VSB -Ch4 .0000V

[illegible] Devices
[illegible]
[illegible] Bell

Segmented Beam Devices

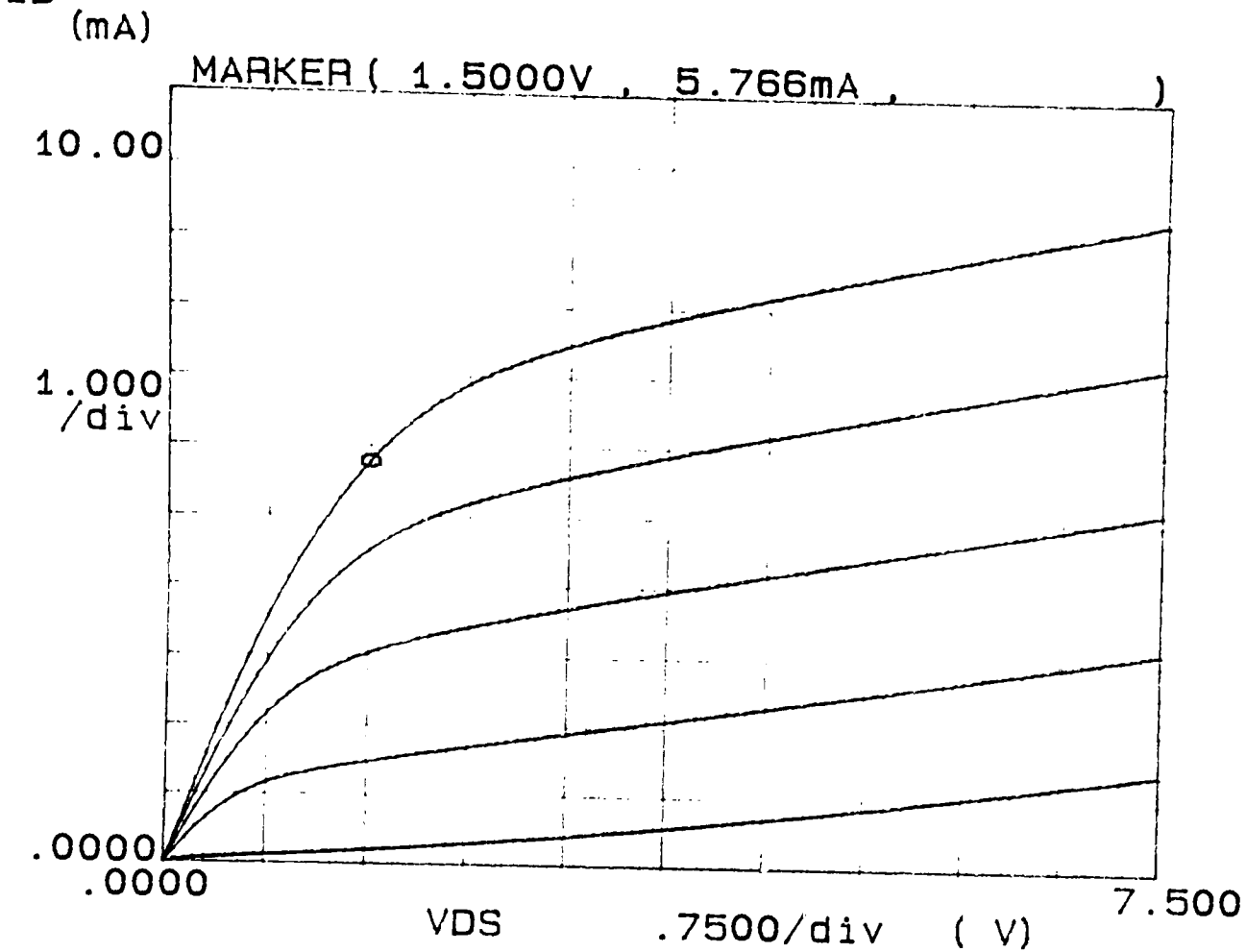
Wafer Location	L=W [illegible] um	Vto	gm (max) I gm/Ohms	VL Vsub=0	VL Vsub=-4	Body Effect VG Vsub=-3
24 23	[illegible]	-0.629	0.908	[illegible]	[illegible]	
26 23	[illegible]	-0.645	0.910	[illegible]		1.0?
38 23	[illegible]	-0.728	0.829	[illegible]	[illegible]	
27 24	[illegible]	-0.542	0.851	[illegible]	[illegible]	
25 24	[illegible]	-0.684	0.938	[illegible]	[illegible]	
24 25	[illegible]	-0.574	0.842	[illegible]	[illegible]	
26 25	[illegible]	-0.547	0.852	[illegible]	[illegible]	
28 25	[illegible]	-0.805	0.860	[illegible]	[illegible]	
27 26	[illegible]	-0.778	0.858	[illegible]	[illegible]	
25 26	[illegible]	-0.577	0.852	[illegible]	[illegible]	
Mean	[illegible]	-0.651	0.866	[illegible]	[illegible]	1.0?
Std Dev	0.291	0.090	0.037	[illegible]	[illegible]	
Dev %	4.66	-13.87	4.24	[illegible]	[illegible]	
Var	0.057	0.008	0.001	[illegible]	[illegible]	

From regression analysis:

Gamma	Vto
0.004	0.669

****** GRAPHICS PLOT ******

D5, N-CH ENH, POLY 1, SEGMENTED



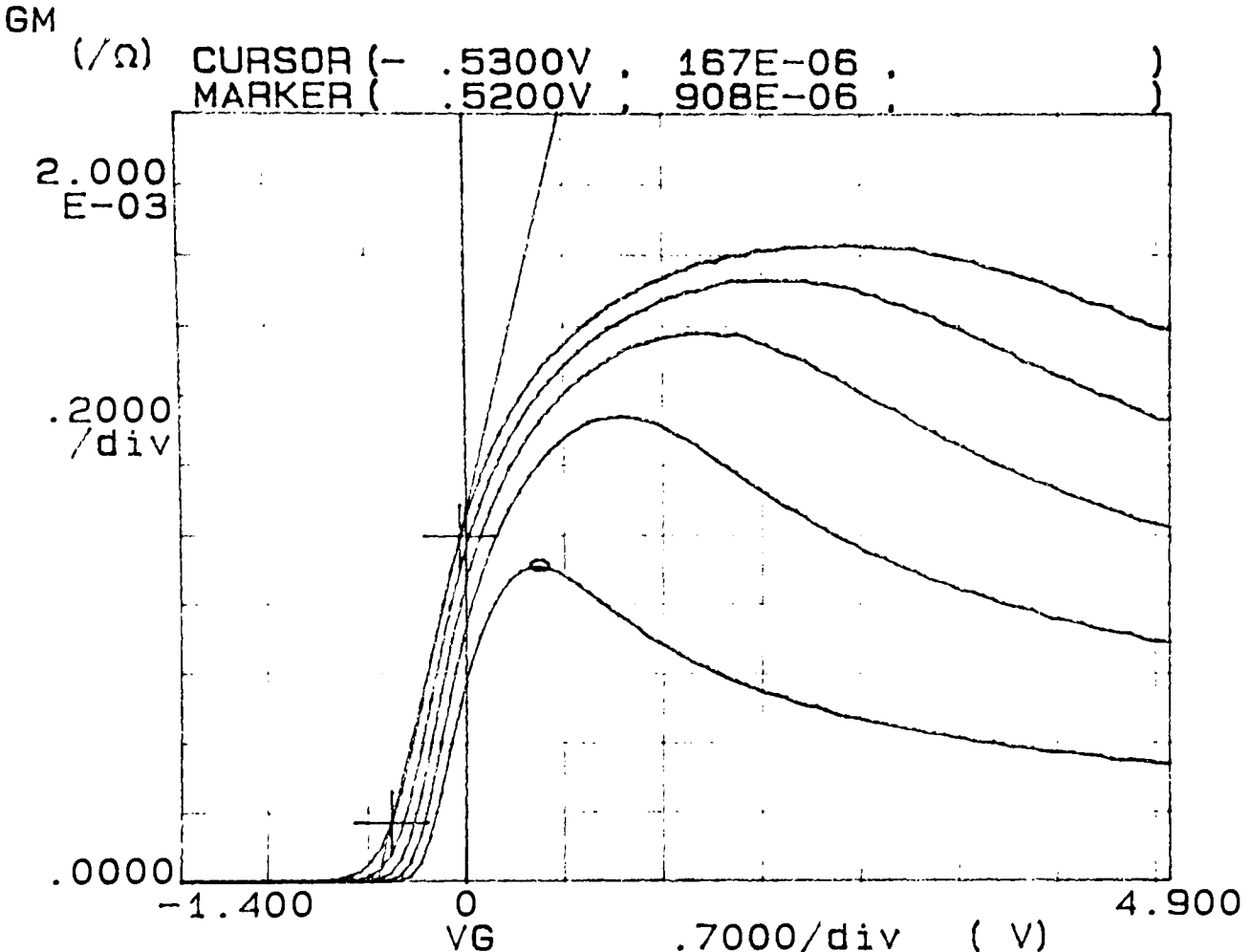
Variable1:
VDS -Ch3
Linear sweep
Start .0000V
Stop 7.5000V
Step .0750V

Variable2:
VG -Ch2
Start .0000V
Stop 4.0000V
Step 1.0000V

Constants:
VS -Ch1 .0000V
VSB -Ch4 .0000V

****** GRAPHICS PLOT ******

D5 N-CH ENH POLY 1 SEGMENTED



	GRAD	1/GRAD	Xintercept	Yintercept
LINE1	1.69E-03	593E+00	-629E-03	1.06E-03
LINE2				

GM (/Ω) = ΔID/ΔVG

Variable1:
VG -Ch2
Linear sweep
Start -2.0000V
Stop 5.0000V
Step .0700V

Variable2:
VD -Ch3
Start .5000V
Stop 2.5000V
Step .5000V

Constants:
VS -Ch1 .0000V
VSB -Ch4 .0000V

Flared Buried Channel Devices

Wafer Location		I-V		gm	Body Effect		
		Idlin	Vto	gm(max)	Vt	V2	V3
		mA		u/Ohms	Vsub=0	Vsub=-4	Vsub=-8
24	23	4.116	-5.77	47.4			
26	23	4.712	-5.75	41.1			
28	23	4.178	-5.88	71.2			
27	24	5.017	-5.77	63.4			
25	24	4.719	-5.86	84.4			
24	25	4.087	-5.86	73.7			
26	25	4.280	-5.84	79.1			
28	26	4.175	-5.90	48.0			
27	26	4.231	-5.82	73.7			
25	26	5.006	-5.88	65.9			
		4.723	-5.1853	64.8			
		0.291	0.075	13.9			
		6.66	-1.28	21.5			
		0.079	0.006	195.8			

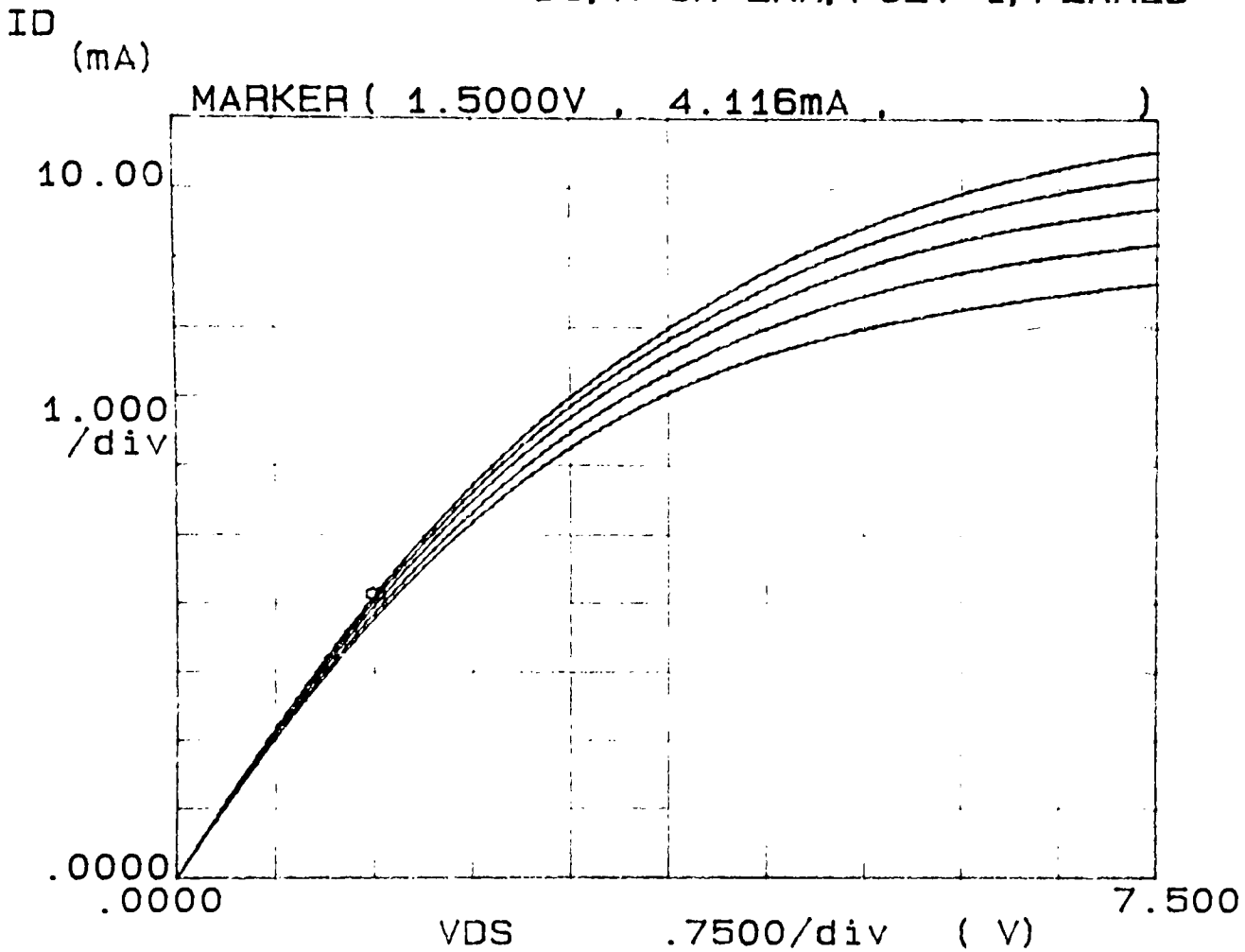
Abnormal curve shapes:

From regression analysis:

Gamma	Vto
0.064	0.659

****** GRAPHICS PLOT ******

D5, N-CH ENH, POLY 1, FLARED



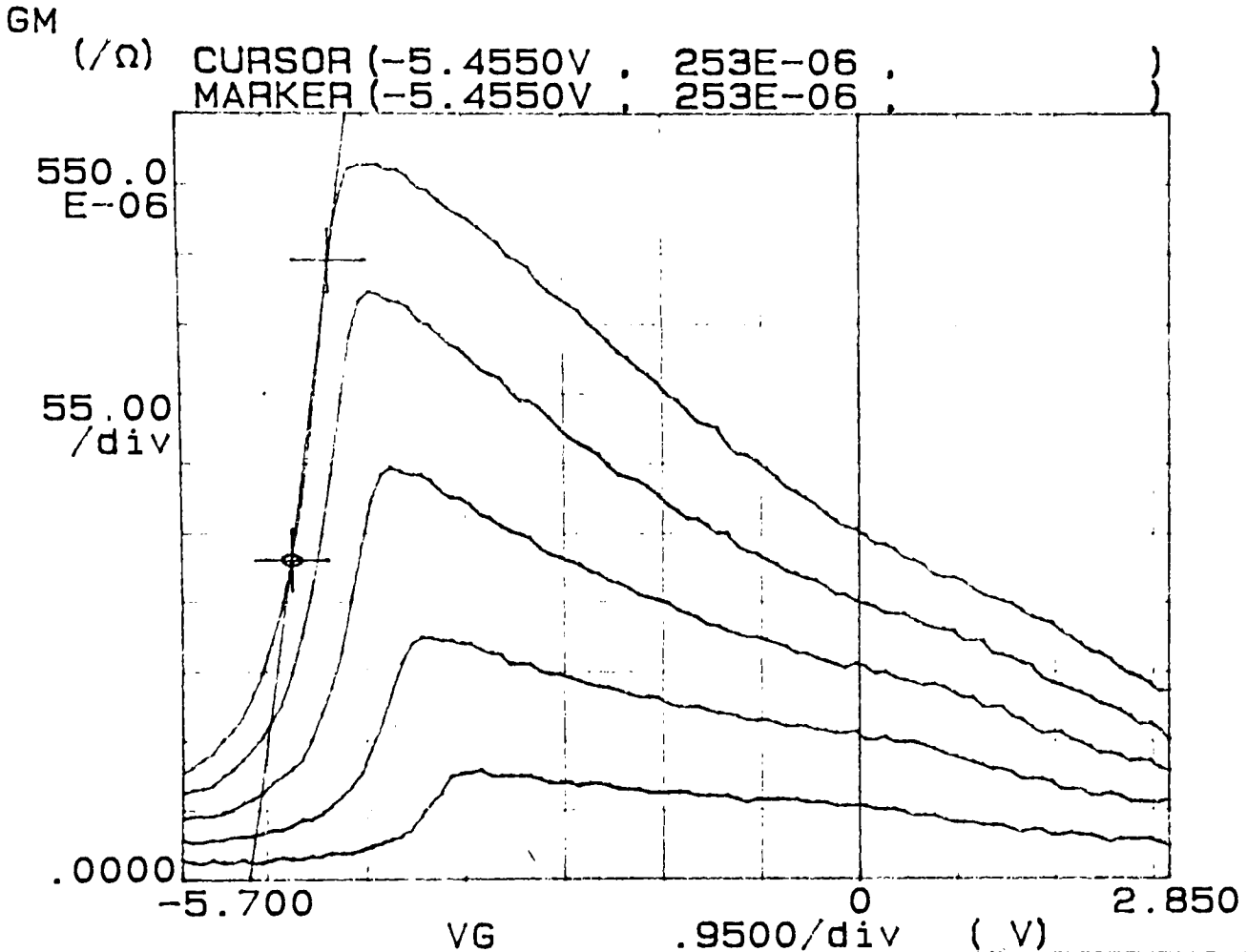
Variable1:
VDS -Ch3
Linear sweep
Start .0000V
Stop 7.5000V
Step .0750V

Variable2:
VG -Ch2
Start .0000V
Stop 4.0000V
Step 1.0000V

Constants:
VS -Ch1 .0000V
VSB -Ch4 .0000V

****** GRAPHICS PLOT ******

D5 N-CH ENH POLY 1 FLARED



Variable1:
VG -Ch2
Linear sweep
Start -6.5000V
Stop 3.0000V
Step .0950V

Variable2:
VD -Ch3
Start .5000V
Stop 2.5000V
Step .5000V

Constants:
VS -Ch1 .0000V
VSB -Ch4 .0000V

	GRAD	1/GRAD	Xintercept	Yintercept
LINE1	622E-06	1.61E+03	-5.86E+00	3.65E-03
LINE2				

GM (/Ω) = ΔID/ΔVG

APPENDIX B

CMOS PROCESS CHARACTERIZATION TRANSISTOR DATA

55 Devices
9/85
C S Bell

T2 n-channel 80u x 6u

Wafer D83-16 Location	I-V i @4.5v mA	Vto	gm gm(max1) u/Ohms	@V	V @300uA	Body Effect Vt Vsub=0	V2 Vsub=2	V3 Vsub=4
23 23	2.626	0.529	285	1.45	1.932	0.524	0.912	1.07
25 23	2.560	0.530	281	1.40	1.952	0.530	0.927	1.11
27 23	2.409	0.561	269	1.50	2.028	0.554	0.943	1.14
26 24	2.473	0.549	274	1.50	1.995	0.536	0.942	1.12
24 24	2.548	0.530	279	1.50	1.958	0.528	0.911	1.08
23 25	2.622	0.535	286	1.35	1.924	0.517	0.893	1.06
25 25	2.573	0.534	281	1.40	1.943	0.522	0.953	1.14
27 25	2.411	0.561	268	1.50	2.025	0.586	1.010	1.21
26 26	2.450	0.537	270	1.50	1.998	0.527	0.995	1.19
24 26	2.241	0.584	252	1.55	2.102	0.531	0.932	1.11
Avg	2.491	0.545	275	1.47	1.986	0.536	0.942	1.12
Std Dev	0.113	0.017	9.729	0.059	0.052	0.019	0.035	0.046
Dev %	4.54	3.20	3.54	4.05	2.64	3.61	3.70	4.14
Var	0.013	.000	94.650	0.004	0.003	.000	0.001	0.002

From regression analysis:

Gamma	Vto	Corr. fit
-0.22324	0.530	0.976

Other parameters:

Phi f	0.258351
Nsub	4.0E+14
un	760

T2 n-channel 80u x 6u

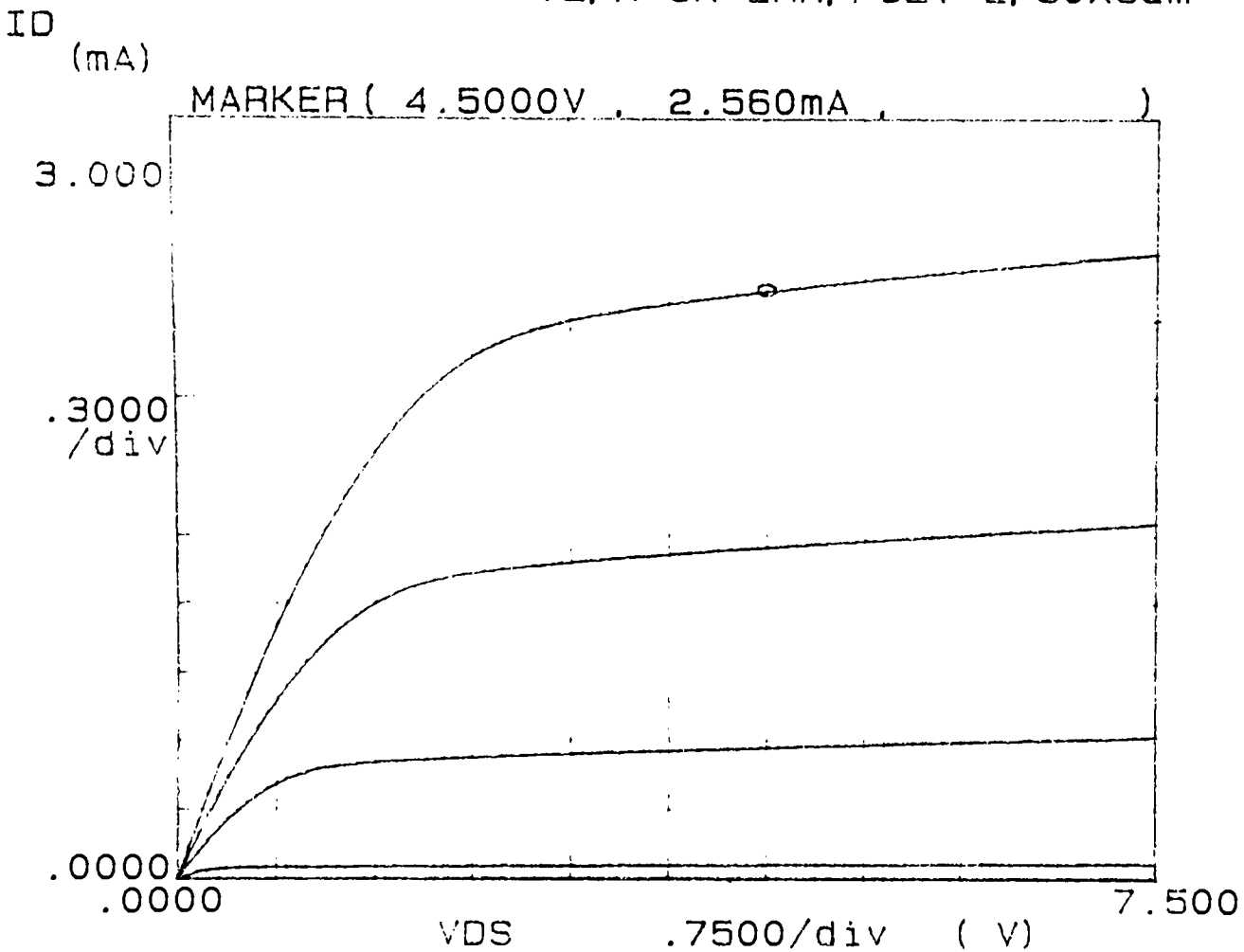
Wafer D83-19 Location	Vt	i @ Vt mA	Body Effect Vt Vsub=0	Body Effect V2 Vsub=-1	Beta	^Beta (grad)
22 22	0.723	1.170	0.721	1.17	2.02E-04	0.0142
23 22	0.737	0.958	0.725	1.18	1.96E-04	0.0140
24 22	0.736	1.060	0.738	1.20	1.85E-04	0.0136
25 22	0.771	0.973	0.766	1.23	1.80E-04	0.0134
26 22	0.781	0.914	0.777	1.25	1.72E-04	0.0131
27 22	0.802	0.951	0.798	1.29	1.72E-04	0.0131
28 22	0.847	0.989	0.843	1.34	1.69E-04	0.0130
28 23	0.855	0.950	0.853	1.35	1.64E-04	0.0128
28 24	0.828	0.970	0.826	1.33	1.61E-04	0.0127
27 24	0.808	0.945	0.803	1.30	1.64E-04	0.0128
25 24	0.743	0.981	0.740	1.20	1.82E-04	0.0135
24 24	0.730	0.972	0.725	1.19	1.88E-04	0.0137
23 24	0.724	0.988	0.716	1.17	1.93E-04	0.0139
22 24	0.719	0.951	0.708	1.16	1.93E-04	0.0139
22 25	0.748	0.968	0.720	1.18	1.88E-04	0.0137
22 26	0.745	0.977	0.717	1.18	1.85E-04	0.0136
23 26	0.729	0.976	0.726	1.19	1.82E-04	0.0135
24 26	0.756	0.976	0.748	1.22	1.80E-04	0.0134
25 26	0.772	0.967	0.765	1.25	1.72E-04	0.0131
26 26	0.804	0.975	0.799	1.29	1.64E-04	0.0128
27 26	0.832	0.988	0.830	1.34	1.59E-04	0.0126
28 26	0.846	0.974	0.846	1.36	1.59E-04	0.0126
Avg	0.774	0.981	0.768	1.244	1.78E-04	0.013
Std Dev	0.045	0.049	0.048	0.067	1.26E-05	.000
Dev %	5.77	4.96	6.23	5.38	7.07	3.55
Var	0.002	0.002	0.002	0.004	.000	.000

From regression analysis:

Gamma	Vto	Corr. fit
-0.339	0.768	0.944

****** GRAPHICS PLOT ******

T2. N-CH ENH. POLY 2. 80X6um



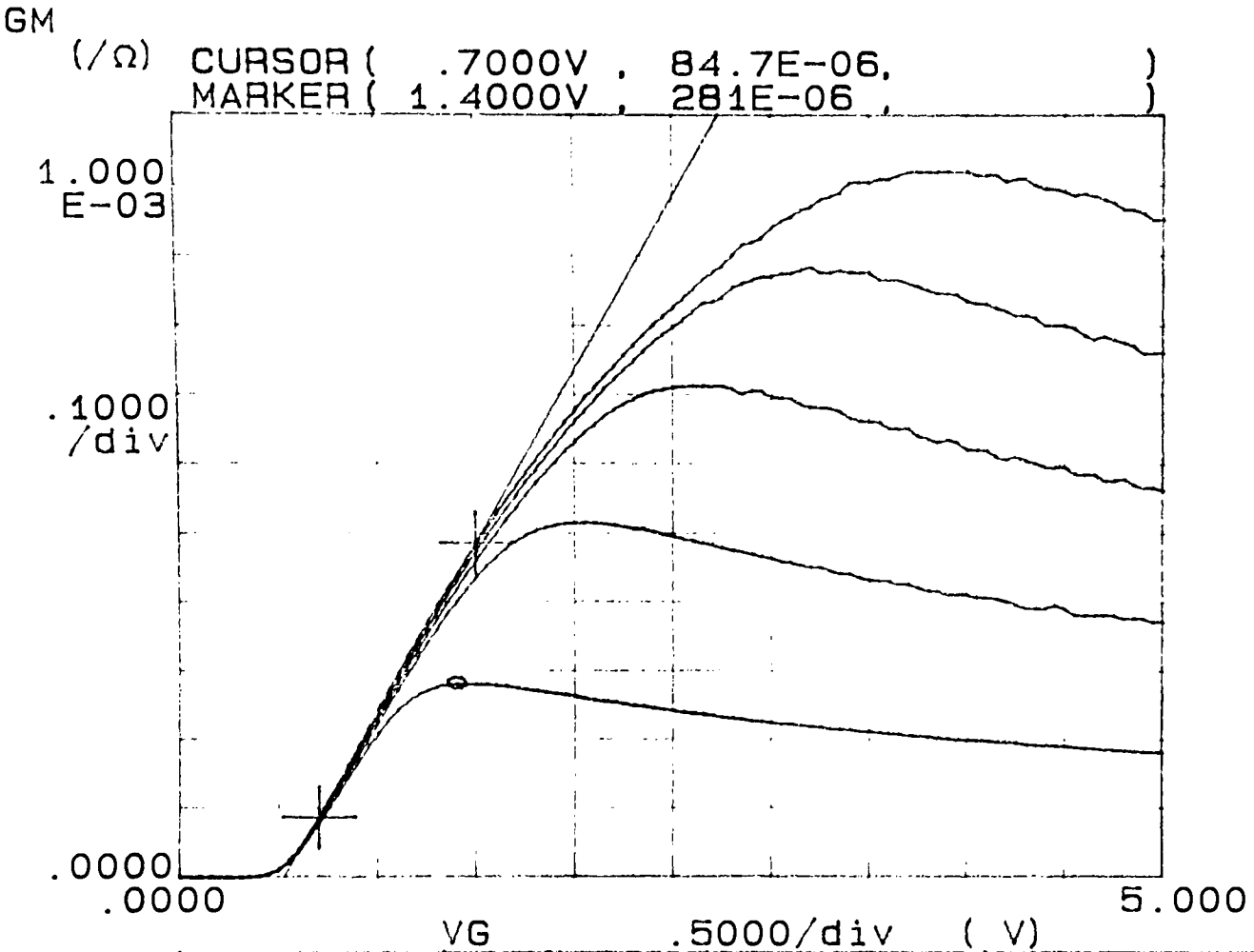
Variable1:
VDS -Ch3
Linear sweep
Start .0000V
Stop 7.5000V
Step .0750V

Variable2:
VG -Ch2
Start .0000V
Stop 4.0000V
Step 1.0000V

Constants:
VS -Ch1 .0000V
VSB -Ch4 .0000V

****** GRAPHICS PLOT ******

T2 N-CH ENH POLY 2 80X6uM



	GRAD	1/GRAD	Xintercept	Yintercept
LINE1	499E-06	2.00E+03	530E-03	-265E-06
LINE2				

GM (/Ω) = ΔID/ΔVG

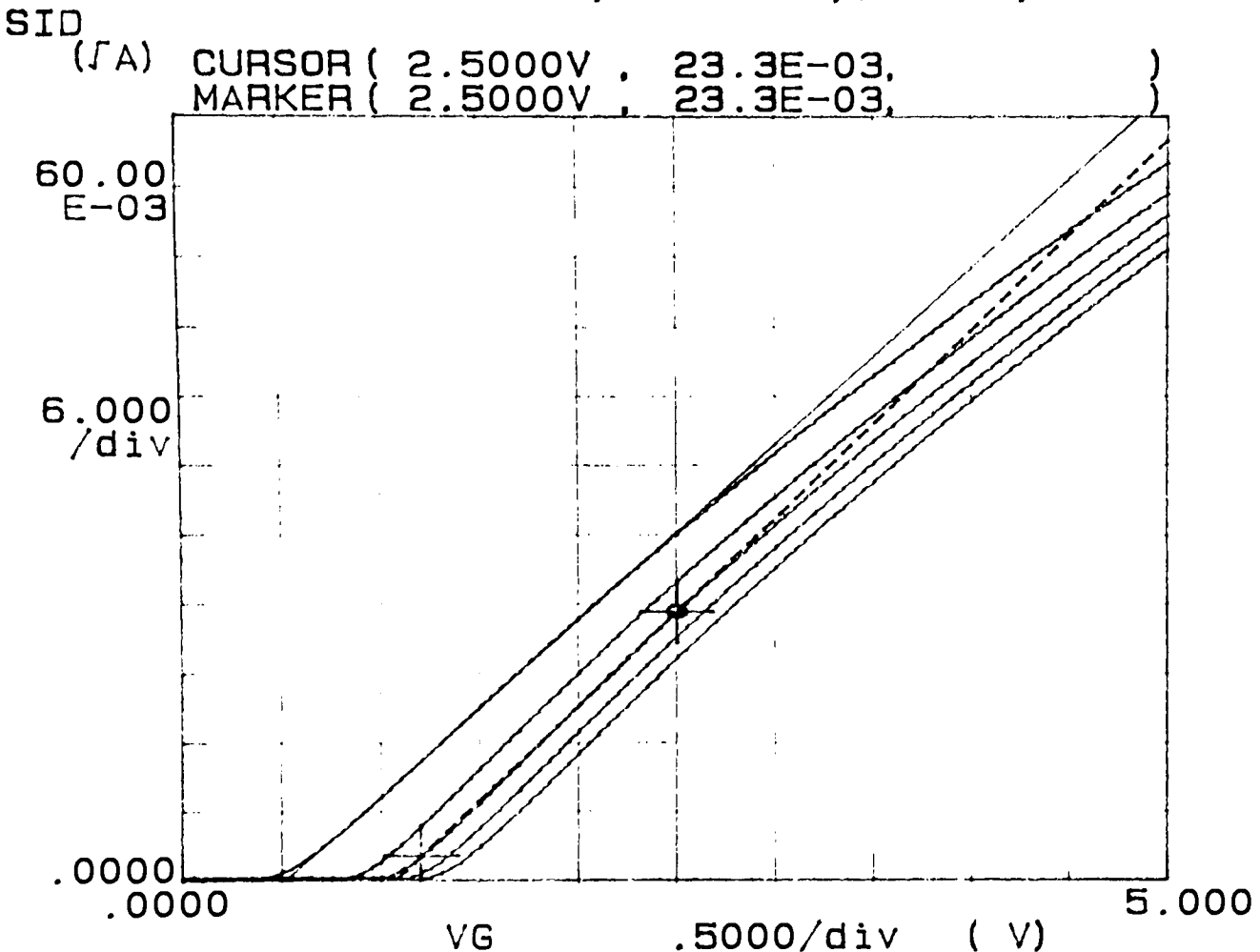
Variable1:
VG -Ch2
Linear sweep
Start .0000V
Stop 5.0000V
Step .0500V

Variable2:
VD -Ch3
Start .5000V
Stop 2.5000V
Step .5000V

Constants:
VS -Ch1 .0000V
VSB -Ch4 .0000V

****** GRAPHICS PLOT ******

T2, N-CH ENH, POLY 2, 80X6um



Variable1:
VG -Ch2
Linear sweep
Start .0000V
Stop 5.0000V
Step .0500V

Variable2:
VSB -Ch4
Start .0000V
Stop -8.0000V
Step -2.0000V

Constants:
VS -Ch1 .0000V

	GRAD	1/GRAD	Xintercept	Yintercept
LINE1	15.3E-03	65.6E+00	524E-03	-7.99E-03
LINE2	16.3E-03	61.4E+00	1.07E+00	-17.5E-03

SID (ΓA) = ΓID

```
*******02/09/86 ********  SPICE 2G.5 (10AUG81)  ********16:07:10*****

         IDS VS VDS FOR THE EK NMOS T26 TRANSISTORS

****     INPUT LISTING                          TEMPERATURE =   27.000 DEG C

******************************************************************************


*                  C S BELL
*
VSUB 9 0 DC 0
VDS 20 0
VGS1 1 0 DC 0
VGS2 2 0 DC 1
VGS3 3 0 DC 2
VGS4 4 0 DC 3
VGS5 5 0 DC 4
M1 11 1 0 9 T26 L=6U W=80U NRS=.1 NRD=.1 AD=1280P AS=1280P PD=192U
+PS=192U
M2 12 2 0 9 T26 L=6U W=80U NRS=.1 NRD=.1 AD=1280P AS=1280P PD=192U
+PS=192U
M3 13 3 0 9 T26 L=6U W=80U NRS=.1 NRD=.1 AD=1280P AS=1280P PD=192U
+PS=192U
M4 14 4 0 9 T26 L=6U W=80U NRS=.1 NRD=.1 AD=1280P AS=1280P PD=192U
+PS=192U
M5 15 5 0 9 T26 L=6U W=80U NRS=.1 NRD=.1 AD=1280P AS=1280P PD=192U
+PS=192U
VID1 20 11 0
VID2 20 12 0
VID3 20 13 0
VID4 20 14 0
VID5 20 15 0

 .MODEL T26 NMOS LAMBDA=.01750 UO=610 TPG=1 TOX=.0711U
+XJ=.5U NSUB=4.008E14 RSH=48.92 PB=.871 CGSO=2.91E-10
+CGDO=2.91E-10 CJ=1.77E-4 MJ=.5 CJSW=8.85E-11 MJSW=.3
+LD=.2U LEVEL=2 VTO=.53 CAMMA=.2232 NSS=4.758E11

 .MODEL T280 NMOS LAMBDA=.00155 UO=610 TPC=1 TOX=.0711U
+XJ=.5U NSUB=4.008E14 RSH=48.92 PB=.871 CGSO=2.91E-10
+CGDO=2.91E-10 CJ=1.77E-4 MJ=.5 CJSW=8.85E-11 MJSW=.3
+LD=.2U LEVEL=2 VTO=.604 GAMMA=.2509 NSS=4.983E11
+
 .MODEL T46 PMOS LAMBDA=.03181 UO=595 TPG=-1 TOX=.0711U
+XJ=1U NSUB=3.695E15 RSH=285.6 PB=.719 CGSO=4.85E-10
+CGDO=4.85E-10 CJ=.958E-5 MJ=.5 CJSW=.958E-11 MJSW=.3
+LD=.6U LEVEL=2 VTO=-1.070 GAMMA=.6645 NSS=1.291E11
+
 .MODEL T480 PMOS LAMBDA=.00184 UO=957 TPG=-1 TOX=.0711U
+XJ=1U NSUB=3.695E15 RSH=285.6 PB=.719 CGSO=4.85E-12
+CGDO=4.85E-12 CJ=.958E-5 MJ=.5 CJSW=.958E-11 MJSW=.3
+LD=.6U LEVEL=2 VTO=-1.009 GAMMA=.7736 NSS=1.478E11
 .WIDTH OUT=80
 .OP
 .DC VDS 0 7.5 .183
 .PLOT DC I(VID5) I(VID4) I(VID3) I(VID2) I(VID1)
+(0,3.3E-3)
 .PRINT DC I(VID5) I(VID4) I(VID3)
 .END
```

IDS VS VDS FOR THE EK NMOS T26 TRANSISTORS

**** MOSFET MODEL PARAMETERS TEMPERATURE = 27.000 DEG C

****

	T26	T280	T46	T480
TYPE	NMOS	NMOS	PMOS	PMOS
LEVEL	2.000	2.000	2.000	2.000
VTO	0.530	0.604	-1.070	-1.009
KP	2.96D-05	2.96D-05	2.89D-05	4.65D-05
GAMMA	0.223	0.251	0.665	0.774
PHI	0.529	0.529	0.644	0.644
LAMBDA	1.75D-02	1.55D-03	3.18D-02	1.84D-03
PB	0.871	0.871	0.719	0.719
CGSO	2.91D-10	2.91D-10	4.85D-10	4.85D-12
CGDO	2.91D-10	2.91D-10	4.85D-10	4.85D-12
RSH	48.920	48.920	285.600	285.600
CJ	1.77D-04	1.77D-04	9.58D-06	9.58D-06
MJ	0.500	0.500	0.500	0.500
CJSW	8.85D-11	8.85D-11	9.58D-12	9.58D-12
MJSW	0.300	0.300	0.300	0.300
TOX	7.11D-08	7.11D-08	7.11D-08	7.11D-08
NSUB	4.01D+14	4.01D+14	3.69D+15	3.69D+15
NSS	4.76D+11	4.98D+11	1.29D+11	1.48D+11
TPG	1.000	1.000	-1.000	-1.000
XJ	5.00D-07	5.00D-07	1.00D-06	1.00D-06
LD	2.00D-07	2.00D-07	6.00D-07	6.00D-07
UO	610.000	610.000	595.000	957.000

*******02/09/86 ******** SPICE 2G.5 (10AUG81) ********16:07:10*****

. IDS VS VDS FOR THE EK NMOS T26 TRANSISTORS

**** DC TRANSFER CURVES TEMPERATURE = 27.000 DEG C

****

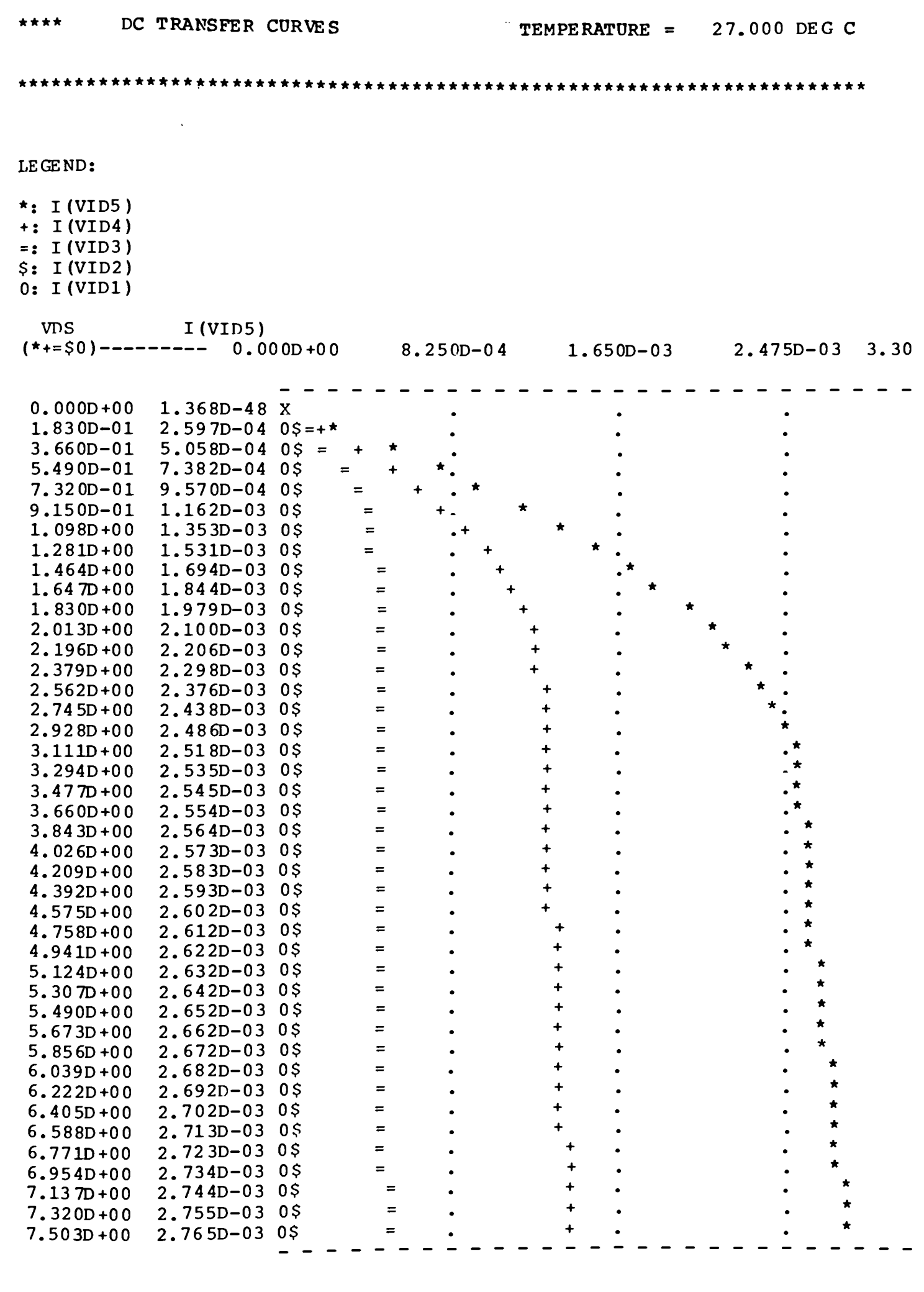
VDS	I(VID5)	I(VID4)	I(VID3)
0.000D+00	1.368D-48	-4.947D-14	-3.867D-13
1.830D-01	2.597D-04	1.839D-04	1.074D-04
3.660D-01	5.058D-04	3.535D-04	1.999D-04
5.490D-01	7.382D-04	5.089D-04	2.776D-04
7.320D-01	9.570D-04	6.500D-04	3.403D-04
9.150D-01	1.162D-03	7.768D-04	3.882D-04
1.098D+00	1.353D-03	8.892D-04	4.210D-04
1.281D+00	1.531D-03	9.871D-04	4.386D-04
1.464D+00	1.694D-03	1.070D-03	4.427D-04
1.647D+00	1.844D-03	1.139D-03	4.446D-04
1.830D+00	1.979D-03	1.193D-03	4.465D-04
2.013D+00	2.100D-03	1.232D-03	4.484D-04
2.196D+00	2.206D-03	1.255D-03	4.502D-04
2.379D+00	2.298D-03	1.264D-03	4.521D-04
2.562D+00	2.376D-03	1.269D-03	4.539D-04
2.745D+00	2.438D-03	1.274D-03	4.558D-04
2.928D+00	2.486D-03	1.279D-03	4.576D-04
3.111D+00	2.518D-03	1.284D-03	4.595D-04
3.294D+00	2.535D-03	1.289D-03	4.614D-04
3.477D+00	2.545D-03	1.294D-03	4.632D-04
3.660D+00	2.554D-03	1.299D-03	4.651D-04
3.843D+00	2.564D-03	1.304D-03	4.669D-04
4.026D+00	2.573D-03	1.309D-03	4.688D-04
4.209D+00	2.583D-03	1.314D-03	4.707D-04
4.392D+00	2.593D-03	1.319D-03	4.725D-04
4.575D+00	2.602D-03	1.324D-03	4.744D-04
4.758D+00	2.612D-03	1.329D-03	4.763D-04
4.941D+00	2.622D-03	1.334D-03	4.782D-04
5.124D+00	2.632D-03	1.339D-03	4.801D-04
5.307D+00	2.642D-03	1.344D-03	4.820D-04
5.490D+00	2.652D-03	1.349D-03	4.840D-04
5.673D+00	2.662D-03	1.355D-03	4.859D-04
5.856D+00	2.672D-03	1.360D-03	4.878D-04
6.039D+00	2.682D-03	1.365D-03	4.898D-04
6.222D+00	2.692D-03	1.370D-03	4.917D-04
6.405D+00	2.702D-03	1.376D-03	4.937D-04
6.588D+00	2.713D-03	1.381D-03	4.957D-04
6.771D+00	2.723D-03	1.386D-03	4.977D-04
6.954D+00	2.734D-03	1.392D-03	4.997D-04
7.137D+00	2.744D-03	1.397D-03	5.017D-04
7.320D+00	2.755D-03	1.403D-03	5.037D-04
7.503D+00	2.765D-03	1.408D-03	5.058D-04

**** DC TRANSFER CURVES TEMPERATURE = 27.000 DEG C

****

LEGEND:

*: I(VID5)
+: I(VID4)
=: I(VID3)
$: I(VID2)
0: I(VID1)



0.000D+00	1.368D-48	X
1.830D-01	2.597D-04	0$=+*
3.660D-01	5.058D-04	0$ = + *
5.490D-01	7.382D-04	0$ = + *
7.320D-01	9.570D-04	0$ = + *
9.150D-01	1.162D-03	0$ = + *
1.098D+00	1.353D-03	0$ = + *
1.281D+00	1.531D-03	0$ = + *
1.464D+00	1.694D-03	0$ = + *
1.647D+00	1.844D-03	0$ = + *
1.830D+00	1.979D-03	0$ = + *
2.013D+00	2.100D-03	0$ = + *
2.196D+00	2.206D-03	0$ = + *
2.379D+00	2.298D-03	0$ = + *
2.562D+00	2.376D-03	0$ = + *
2.745D+00	2.438D-03	0$ = + *
2.928D+00	2.486D-03	0$ = + *
3.111D+00	2.518D-03	0$ = + *
3.294D+00	2.535D-03	0$ = + *
3.477D+00	2.545D-03	0$ = + *
3.660D+00	2.554D-03	0$ = + *
3.843D+00	2.564D-03	0$ = + *
4.026D+00	2.573D-03	0$ = + *
4.209D+00	2.583D-03	0$ = + *
4.392D+00	2.593D-03	0$ = + *
4.575D+00	2.602D-03	0$ = + *
4.758D+00	2.612D-03	0$ = + *
4.941D+00	2.622D-03	0$ = + *
5.124D+00	2.632D-03	0$ = + *
5.307D+00	2.642D-03	0$ = + *
5.490D+00	2.652D-03	0$ = + *
5.673D+00	2.662D-03	0$ = + *
5.856D+00	2.672D-03	0$ = + *
6.039D+00	2.682D-03	0$ = + *
6.222D+00	2.692D-03	0$ = + *
6.405D+00	2.702D-03	0$ = + *
6.588D+00	2.713D-03	0$ = + *
6.771D+00	2.723D-03	0$ = + *
6.954D+00	2.734D-03	0$ = + *
7.137D+00	2.744D-03	0$ = + *
7.320D+00	2.755D-03	0$ = + *
7.503D+00	2.765D-03	0$ = + *

*******02/09/86 ******** SPICE 2G.5 (10AUG81) ********16:07:10*****

IDS VS VDS FOR THE EK NMOS T26 TRANSISTORS

**** OPERATING POINT INFORMATION TEMPERATURE = 27.000 DEG C

****

**** MOSFETS

	M1	M2	M3	M4	M5
MODEL	T26	T26	T26	T26	T26
ID	0.00D+00	0.00D+00	1.19D-22	9.16D-24	3.16D-33
VGS	0.000	1.000	2.000	3.000	4.000
VDS	0.000	0.000	0.000	0.000	0.000
VBS	0.000	0.000	0.000	0.000	0.000
VTH	0.508	0.508	0.508	0.508	0.508
VDSAT	0.000	0.442	1.366	2.307	3.256
GM	0.00D+00	0.00D+00	0.00D+00	0.00D+00	0.00D+00
GDS	0.00D+00	2.08D-04	6.31D-04	1.05D-03	1.48D-03
GMB	0.00D+00	0.00D+00	0.00D+00	0.00D+00	0.00D+00
CBD	2.44D-13	2.44D-13	2.44D-13	2.44D-13	2.44D-13
CBS	2.44D-13	2.44D-13	2.44D-13	2.44D-13	2.44D-13
CGSOVL	2.33D-14	2.33D-14	2.33D-14	2.33D-14	2.33D-14
CGDOVL	2.33D-14	2.33D-14	2.33D-14	2.33D-14	2.33D-14
CGBOVL	0.00D+00	0.00D+00	0.00D+00	0.00D+00	0.00D+00
CGS	0.00D+00	1.09D-13	1.09D-13	1.09D-13	1.09D-13
CGD	0.00D+00	1.09D-13	1.09D-13	1.09D-13	1.09D-13
CGB	2.09D-13	0.00D+00	0.00D+00	0.00D+00	0.00D+00

JOB CONCLUDED

TOTAL JOB TIME 0.19

D3 Devices
7/85
C S Bell

T2 n-channel 80u x 80u

Wafer D83-19 Location	Vt	i @ Vt mA	Body Effect Vt Vsub=0	V2 Vsub=-1	Beta	^Beta (grad)
22 22	0.781	0.292	0.783	1.24	1.32E-03	0.0363
23 22	0.808	0.227	0.782	1.25	1.11E-03	0.0333
24 22	0.800	0.257	0.796	1.26	1.09E-03	0.0330
25 22	0.828	0.220	0.808	1.29	1.05E-03	0.0324
26 22	0.839	0.240	0.828	1.32	1.02E-03	0.0320
27 22	0.867	0.245	0.853	1.35	1.00E-03	0.0317
28 22	0.910	0.260	0.882	1.39	9.67E-04	0.0311
28 23	0.914	0.273	0.911	1.42	9.67E-04	0.0311
28 24	0.885	0.250	0.883	1.39	9.73E-04	0.0312
27 24	0.859	0.242	0.858	1.36	9.92E-04	0.0315
25 24	0.804	0.294	0.805	1.28	1.06E-03	0.0326
24 24	0.792	0.268	0.786	1.26	1.09E-03	0.0330
23 24	0.784	0.242	0.766	1.24	1.11E-03	0.0333
22 24	0.782	0.262	0.765	1.23	1.12E-03	0.0334
22 25	0.788	0.290	0.778	1.25	1.11E-03	0.0333
22 26	0.789	0.276	0.773	1.24	1.10E-03	0.0331
23 26	0.786	0.263	0.786	1.25	1.08E-03	0.0329
24 26	0.805	0.261	0.801	1.28	1.06E-03	0.0325
25 26	0.829	0.237	0.822	1.31	1.03E-03	0.0321
26 26	0.865	0.257	0.858	1.36	9.86E-04	0.0314
27 26	0.903	0.242	0.881	1.39	9.55E-04	0.0309
28 26	0.900	0.280	0.898	1.41	9.55E-04	0.0309
Avg	0.833	0.258	0.823	1.308	1.05E-03	0.0324
Std Dev	0.046	0.020	0.046	0.063	8.10E-05	0.001
Dev %	5.52	7.76	5.56	4.81	7.70	3.72
Var	0.002	.000	0.002	0.004	6.56E-09	.000

From regression analysis:

Gamma	Vto	Corr. fit
-0.346	0.823	0.951

T2 n-channel 80u x 80u

Wafer D83-16 Location	I-V i @4.5v uA	Vto	gm(max) u/Ohms	gm @V	V @25uA	Body Effect Vt Vsub=0	Vt Vsub=2	Vt Vsub=4
23 23	161.8	0.595	18.2	1.50	2.292	0.559	0.99	1.22
25 23	155.2	0.609	17.8	1.50	2.330	0.602	1.05	1.27
27 23	146.9	0.635	17.1	1.60	2.400	0.623	1.07	1.30
26 24	149.3	0.618	17.3	1.55	2.380	0.620	1.06	1.28
24 24	157.3	0.595	17.9	1.50	2.318	0.591	1.02	1.23
23 25	160.8	0.594	18.3	1.50	2.292	0.587	1.01	1.21
25 25	158.1	0.590	18.1	1.50	2.309	0.618	1.07	1.30
27 25	146.6	0.627	17.3	1.55	2.404	0.666	1.13	1.36
26 26	150.8	0.614	17.5	1.50	2.370	0.649	1.11	1.34
24 26	140.4	0.657	16.7	1.55	2.463	0.612	1.06	1.27
Avg	152.720	0.613	17.620	1.525	2.356	0.613	1.057	1.278
Std Dev	6.651	0.020	0.498	0.034	0.054	0.029	0.041	0.047
Dev %	4.35	3.34	2.82	2.20	2.29	4.75	3.89	3.67
Var	44.230	.000	0.248	0.001	0.003	0.001	0.002	0.002

From regression analysis:

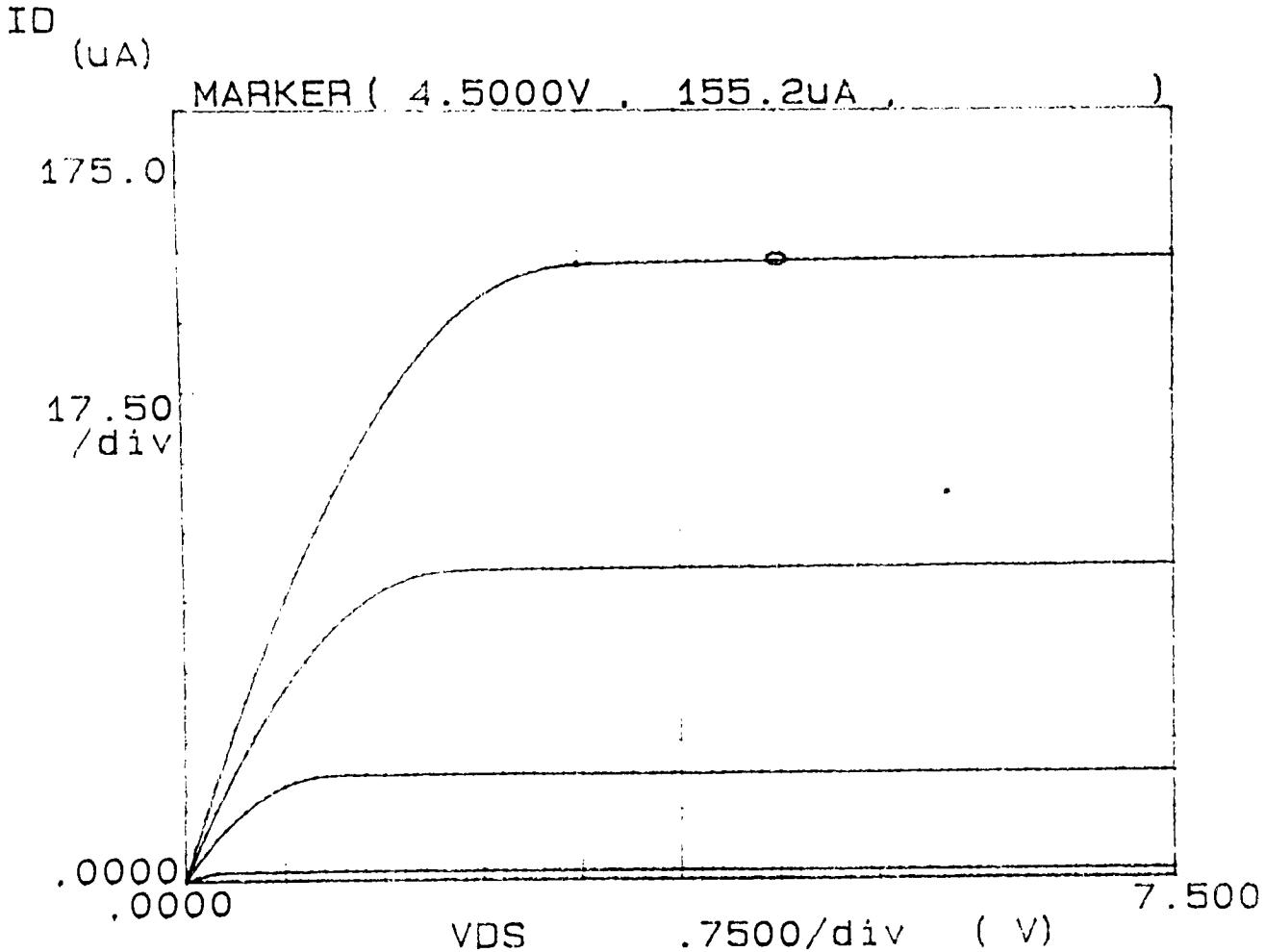
Gamma	Vto	Corr. fit
-0.25090	0.604	0.972

Other parameters:

Phi f	0.258351
Nsub	4.0E+14
un	760

****** GRAPHICS PLOT ******

T2, N-CH ENH, POLY 2, 80X80um



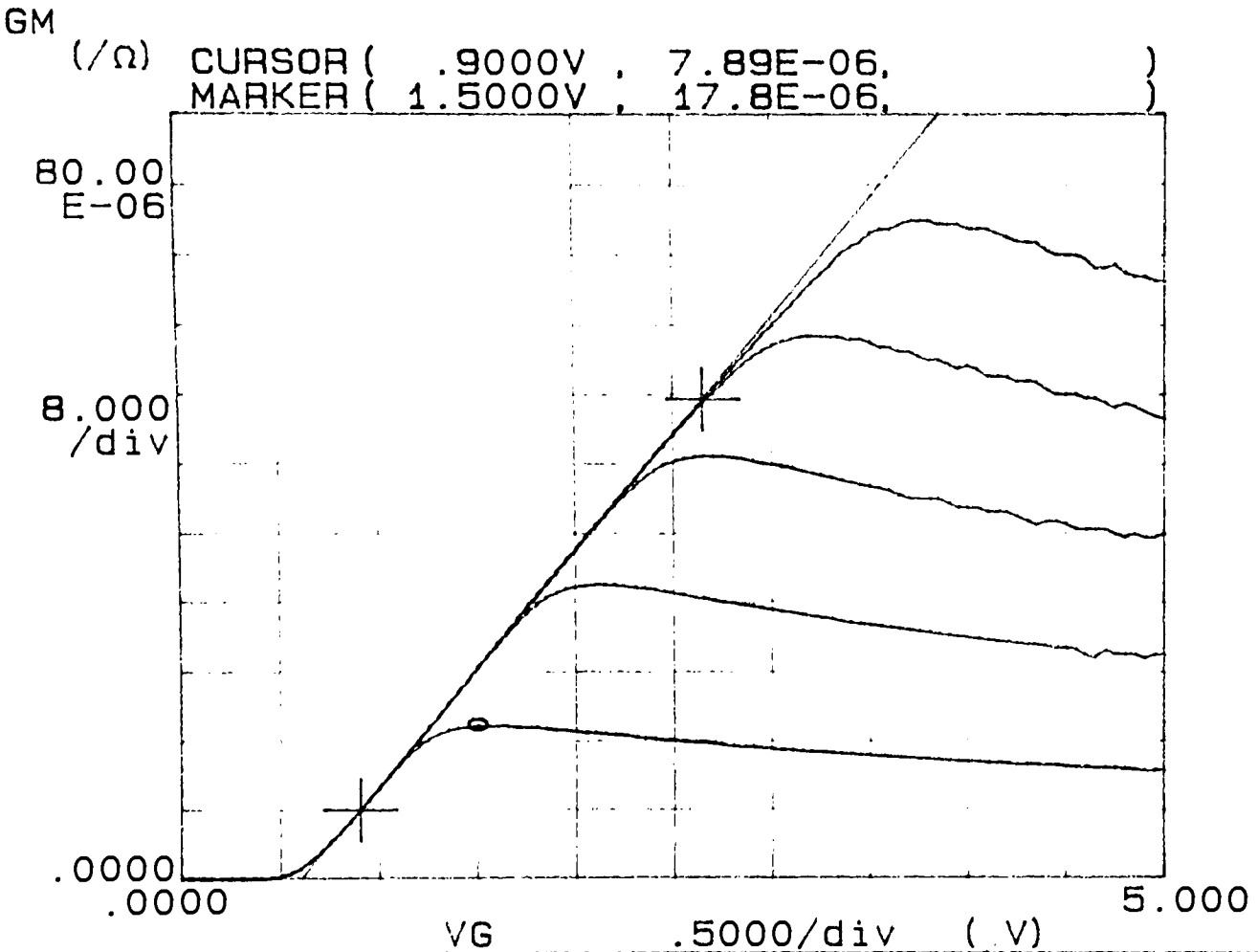
Variable1:
VDS -Ch3
Linear sweep
Start .0000V
Stop 7.5000V
Step .0750V

Variable2:
VG -Ch2
Start .0000V
Stop 4.0000V
Step 1.0000V

Constants:
VS -Ch1 .0000V
VSB -Ch4 .0000V

****** GRAPHICS PLOT ******

T2 N-CH ENH POLY 2 80X80uM



	GRAD	1/GRAD	Xintercept	Yintercept
LINE1	27.1E-06	36.9E+03	609E-03	-16.5E-06
LINE2				

GM (/Ω) = ΔID/ΔVG

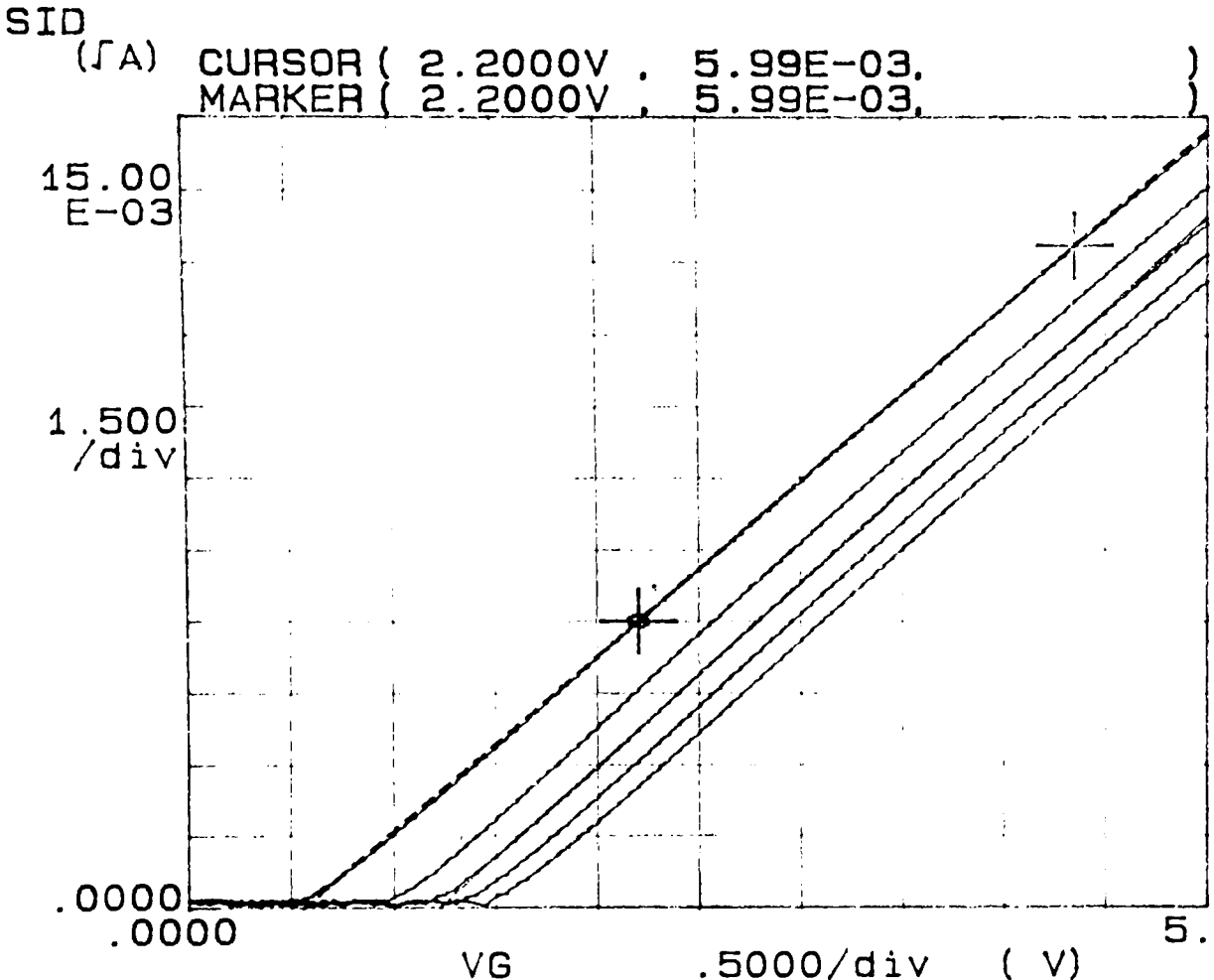
Variable1:
VG -Ch2
Linear sweep
Start .0000V
Stop 5.0000V
Step .0500V

Variable2:
VD -Ch3
Start .5000V
Stop 2.5000V
Step .5000V

Constants:
VS -Ch1 .0000V
VSB -Ch4 .0000V

****** GRAPHICS PLOT ******

T2, N-CH ENH, POLY 2, 80X80um



Variable1:
VG -Ch2
Linear sweep
Start .0000V
Stop 5.0000V
Step .0500V

Variable2:
VSB -Ch4
Start .0000V
Stop -8.0000V
Step -2.0000V

Constants:
VS -Ch1 .0000V

	GRAD	1/GRAD	Xintercept	Yintercept
LINE1	3.81E-03	262E+00	1.22E+00	-4.66E-03
LINE2	3.65E-03	274E+00	559E-03	-2.04E-03

SID (ΓA) = ΓID

```
*******02/09/86 ********  SPICE 2G.5 (10AUG81)  ********16:07:17*****

        IDS VS VDS FOR THE EK NMOS T280 TRANSISTORS

****      INPUT LISTING                          TEMPERATURE =   27.000 DEG C

******************************************************************************


*                  C S BELL
*
VSUB 9 0 DC 0
VDS 20 0
VGS1 1 0 DC 0
VGS2 2 0 DC 1
VGS3 3 0 DC 2
VGS4 4 0 DC 3
VGS5 5 0 DC 4
M1 11 1 0 9 T280 L=80U W=80U NRS=.1 NRD=.1 AD=1280P AS=1280P PD=192U
+PS=192U
M2 12 2 0 9 T280 L=80U W=80U NRS=.1 NRD=.1 AD=1280P AS=1280P PD=192U
+PS=192U
M3 13 3 0 9 T280 L=80U W=80U NRS=.1 NRD=.1 AD=1280P AS=1280P PD=192U
+PS=192U
M4 14 4 0 9 T280 L=80U W=80U NRS=.1 NRD=.1 AD=1280P AS=1280P PD=192U
+PS=192U
M5 15 5 0 9 T280 L=80U W=80U NRS=.1 NRD=.1 AD=1280P AS=1280P PD=192U
+PS=192U
VID1 20 11 0
VID2 20 12 0
VID3 20 13 0
VID4 20 14 0
VID5 20 15 0

 .MODEL T26 NMOS LAMBDA=.02255 UO=680 TPG=1 TOX=.0711U
+XJ=.5U NSUB=4.008E14 RSH=48.92 PB=.871 CGSO=2.91E-10
+CGDO=2.91E-10 CJ=1.77E-4 MJ=.5 CJSW=8.85E-11 MJSW=.3
+LD=.2U LEVEL=2 VTO=.53 GAMMA=.2232 NSS=4.758E11

 .MODEL T280 NMOS LAMBDA=.00155 UO=610 TPG=1 TOX=.0711U
+XJ=.5U NSUB=4.008E14 RSH=48.92 PB=.871 CGSO=2.91E-10
+CGDO=2.91E-10 CJ=1.77E-4 MJ=.5 CJSW=8.85E-11 MJSW=.3
+LD=.2U LEVEL=2 VTO=.604 GAMMA=.2509 NSS=4.983E11
+
 .MODEL T46 PMOS LAMBDA=.03181 UO=210 TPG=-1 TOX=.0711U
+XJ=1U NSUB=3.695E15 RSH=285.6 PB=.719 CGSO=4.85E-10
+CGDO=4.85E-10 CJ=.958E-5 MJ=.5 CJSW=.958E-11 MJSW=.3
+LD=.6U LEVEL=2 VTO=-1.070 GAMMA=.6645 NSS=1.291E11
+
 .MODEL T480 PMOS LAMBDA=.00184 UO=210 TPG=-1 TOX=.0711U
+XJ=1U NSUB=3.695E15 RSH=285.6 PB=.719 CGSO=4.85E-12
+CGDO=4.85E-12 CJ=.958E-5 MJ=.5 CJSW=.958E-11 MJSW=.3
+LD=.6U LEVEL=2 VTO=-1.009 GAMMA=.7736 NSS=1.478E11
 .WIDTH OUT=80
 .OP
 .DC VDS 0 7.5 .183
 .PLOT DC I(VID5) I(VID4) I(VID3) I(VID2) I(VID1)
+(0,192.5E-06)
 .PRINT DC I(VID5) I(VID4) I(VID3)
 .END
```

IDS VS VDS FOR THE EK NMOS T280 TRANSISTORS

**** MOSFET MODEL PARAMETERS TEMPERATURE = 27.000 DEG C

****

	T26	T280	T46	T480
TYPE	NMOS	NMOS	PMOS	PMOS
LEVEL	2.000	2.000	2.000	2.000
VTO	0.530	0.604	-1.070	-1.009
KP	3.30D-05	2.96D-05	1.02D-05	1.02D-05
GAMMA	0.223	0.251	0.665	0.774
PHI	0.529	0.529	0.644	0.644
LAMBDA	2.25D-02	1.55D-03	3.18D-02	1.84D-03
PB	0.871	0.871	0.719	0.719
CGSO	2.91D-10	2.91D-10	4.85D-10	4.85D-12
CGDO	2.91D-10	2.91D-10	4.85D-10	4.85D-12
RSH	48.920	48.920	285.600	285.600
CJ	1.77D-04	1.77D-04	9.58D-06	9.58D-06
MJ	0.500	0.500	0.500	0.500
CJSW	8.85D-11	8.85D-11	9.58D-12	9.58D-12
MJSW	0.300	0.300	0.300	0.300
TOX	7.11D-08	7.11D-08	7.11D-08	7.11D-08
NSUB	4.01D+14	4.01D+14	3.69D+15	3.69D+15
NSS	4.76D+11	4.98D+11	1.29D+11	1.48D+11
TPG	1.000	1.000	-1.000	-1.000
XJ	5.00D-07	5.00D-07	1.00D-06	1.00D-06
LD	2.00D-07	2.00D-07	6.00D-07	6.00D-07
UO	680.000	610.000	210.000	210.000

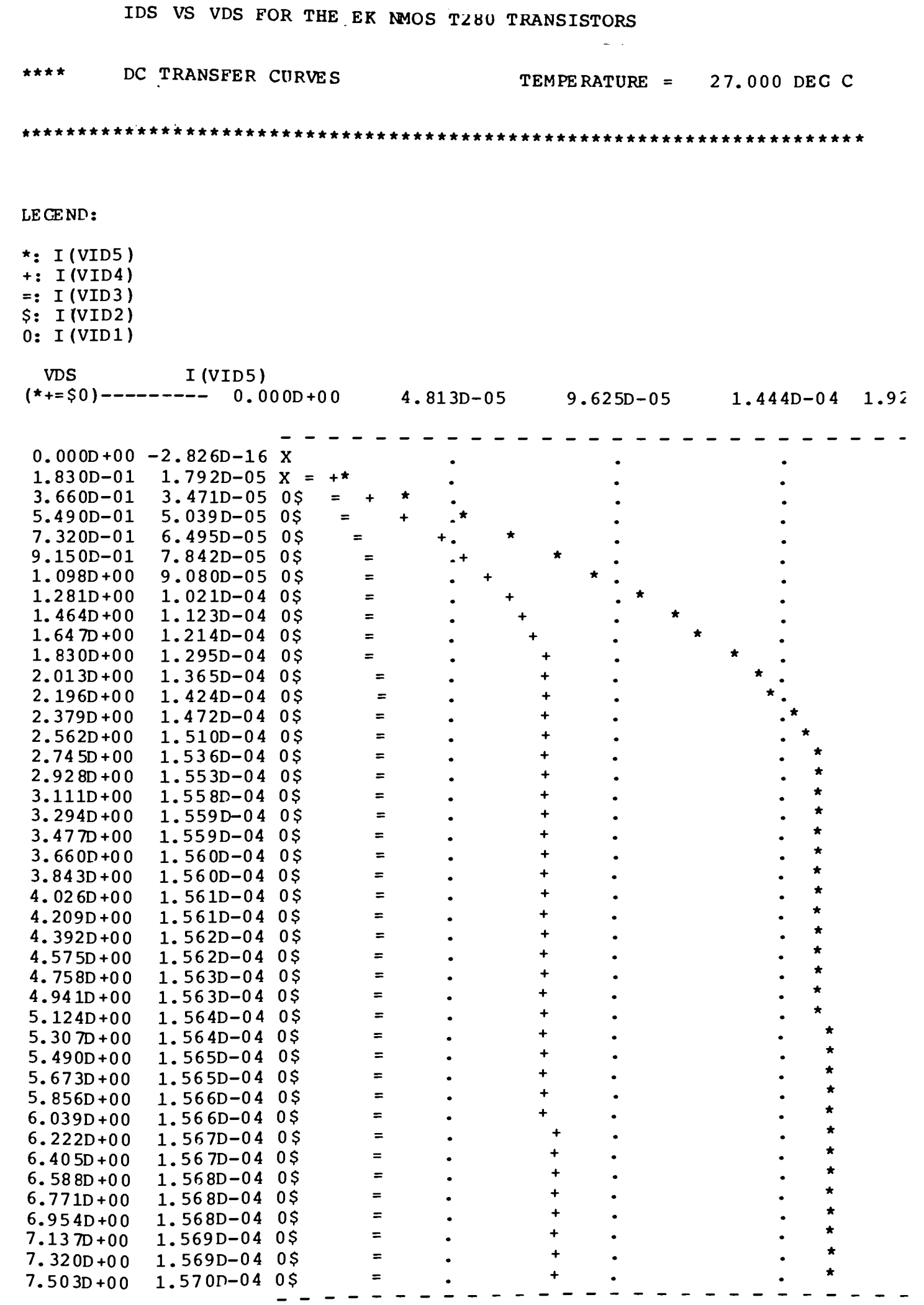
IDS VS VDS FOR THE EK NMOS T280 TRANSISTORS

**** DC TRANSFER CURVES TEMPERATURE = 27.000 DEG C

****

LEGEND:

*: I(VID5)
+: I(VID4)
=: I(VID3)
$: I(VID2)
0: I(VID1)



IDS VS VDS FOR THE EK NMOS T280 TRANSISTORS

**** OPERATING POINT INFORMATION TEMPERATURE = 27.000 DEG C

****

**** MOSFETS

	M1	M2	M3	M4	M5
MODEL	T280	T280	T280	T280	T280
ID	0.00D+00	0.00D+00	2.44D-26	1.96D-25	5.41D-25
VGS	0.000	1.000	2.000	3.000	4.000
VDS	0.000	0.000	0.000	0.000	0.000
VBS	0.000	0.000	0.000	0.000	0.000
VTH	0.602	0.602	0.602	0.602	0.602
VDSAT	0.000	0.346	1.247	2.170	3.105
GM	0.00D+00	0.00D+00	0.00D+00	0.00D+00	0.00D+00
GDS	0.00D+00	1.18D-05	4.16D-05	7.14D-05	1.01D-04
GMB	0.00D+00	0.00D+00	0.00D+00	0.00D+00	0.00D+00
CBD	2.44D-13	2.44D-13	2.44D-13	2.44D-13	2.44D-13
CBS	2.44D-13	2.44D-13	2.44D-13	2.44D-13	2.44D-13
CGSOVL	2.33D-14	2.33D-14	2.33D-14	2.33D-14	2.33D-14
CGDOVL	2.33D-14	2.33D-14	2.33D-14	2.33D-14	2.33D-14
CCBOVL	0.00D+00	0.00D+00	0.00D+00	0.00D+00	0.00D+00
CGS	0.00D+00	1.55D-12	1.55D-12	1.55D-12	1.55D-12
CGD	0.00D+00	1.55D-12	1.55D-12	1.55D-12	1.55D-12
CGB	3.09D-12	0.00D+00	0.00D+00	0.00D+00	0.00D+00

JOB CONCLUDED

TOTAL JOB TIME 0.19

T4 p-channel 80u x 6u

Wafer D83-16 Location	I-V i @4.5v uA	Vto	gm gm(max1) u/Ohms	gm @V	gm V @550uA	Body Effect Vt Vsub=3	Body Effect V2 Vsub=5	Body Effect V3 Vsub=7
23 23	-1.203	-2.04	88.9	-3.00	-4.245	-1.74	-2.07	-2.22
25 23	-1.163	-2.09	88.1	-3.08	-4.863	-1.80	-2.12	-2.38
27 23	-1.073	-2.16	83.1	-3.16	-5.017	-1.84	-2.15	-2.41
26 24	-1.107	-2.15	85.3	-3.16	-4.962	-1.82	-2.13	-2.39
24 24	-1.155	-2.10	85.9	-2.92	-4.870	-1.76	-2.06	-2.31
23 25	-1.195	-2.06	89.2	-3.00	-4.806	-1.74	-2.05	-2.29
25 25	-1.170	-2.08	88.0	-3.08	-4.847	-1.83	-2.15	-2.41
27 25	-1.085	-2.16	84.5	-3.16	-4.996	-1.88	-2.22	-2.50
26 26	-1.079	-2.14	82.7	-3.16	-4.998	-1.86	-2.19	-2.47
24 26	-0.978	-2.21	77.4	-3.16	-5.184	-1.80	-2.12	-2.38
Avg	-1.121	-2.119	85.310	-3.088	-4.879	-1.807	-2.126	-2.376
Std Dev	0.066	0.050	3.440	0.084	0.236	0.046	0.052	0.079
Dev %	5.88	2.38	4.03	2.70	4.83	2.55	2.46	3.34
Var	0.004	0.003	11.831	0.007	0.056	0.002	0.003	0.006

From regression analysis:

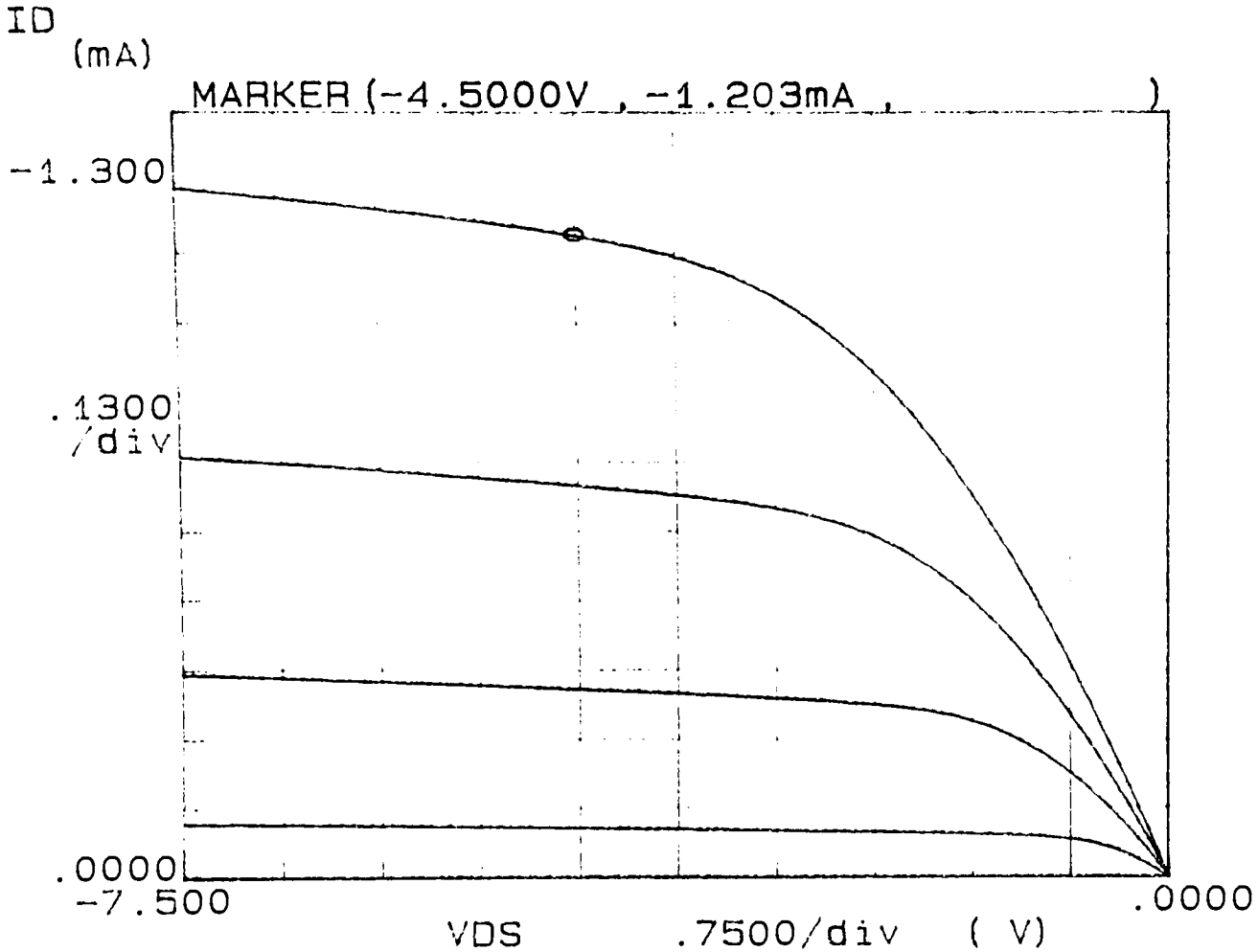
Gamma	Vto
-0.66448	-1.071

Other parameters:

Phi f	0.314388
Nsub	3.7E+15
up	210

****** GRAPHICS PLOT ******

T4, P-CH ENH, POLY 2, 80X6um



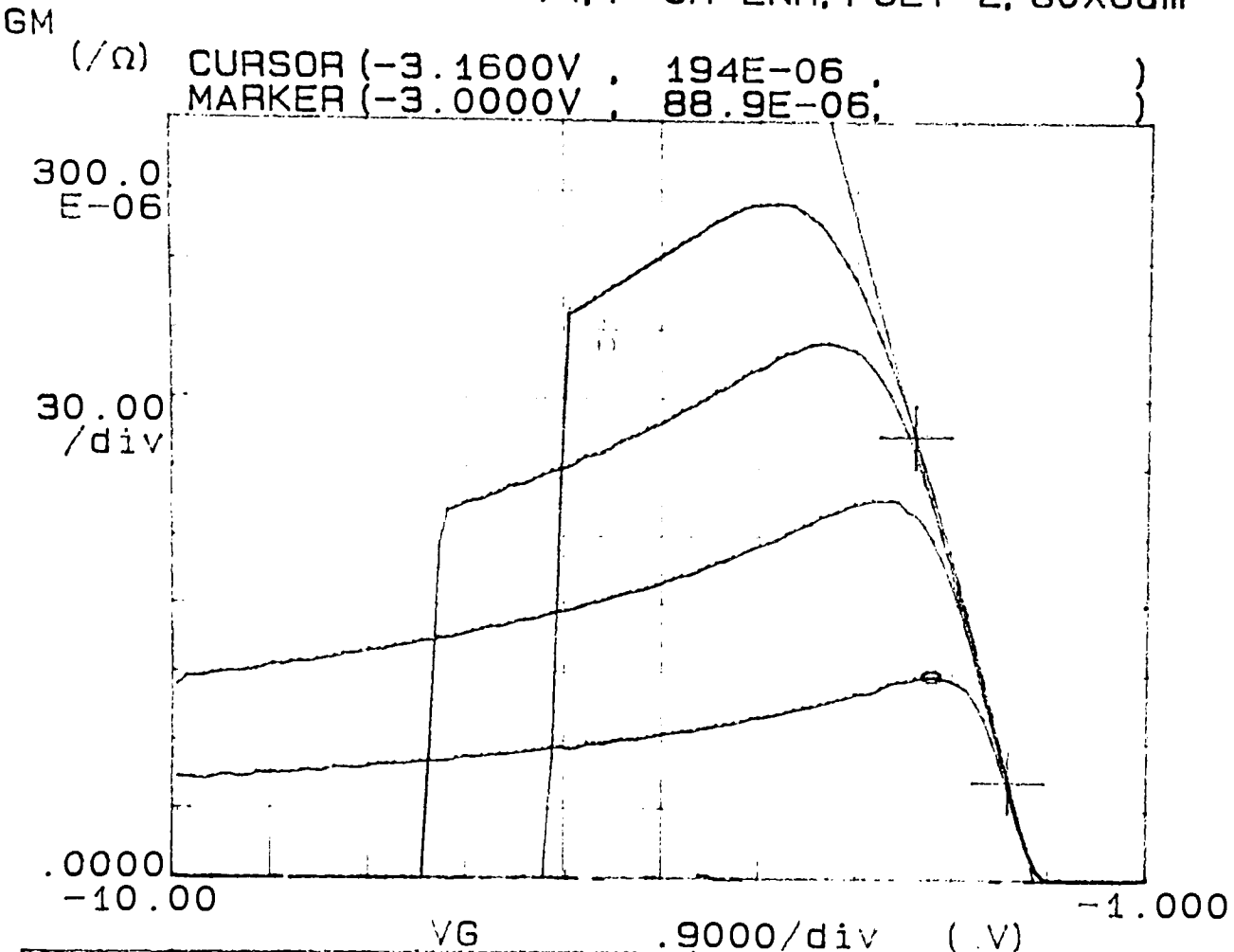
Variable1:
VDS -Ch3
Linear sweep
Start .0000V
Stop -7.5000V
Step - .0750V

Variable2:
VG -Ch2
Start -2.0000V
Stop -6.0000V
Step -1.0000V

Constants:
VS -Ch1 .0000V
VNW -Ch4 5.0000V

****** GRAPHICS PLOT ******

T4. P-CH ENH. POLY 2. 80X6um



Variable1:
VG -Ch2
Linear sweep
Start -1.0000V
Stop -10.000V
Step - .0800V

Variable2:
VD -Ch3
Start .0000V
Stop -2.0000V
Step - .5000V

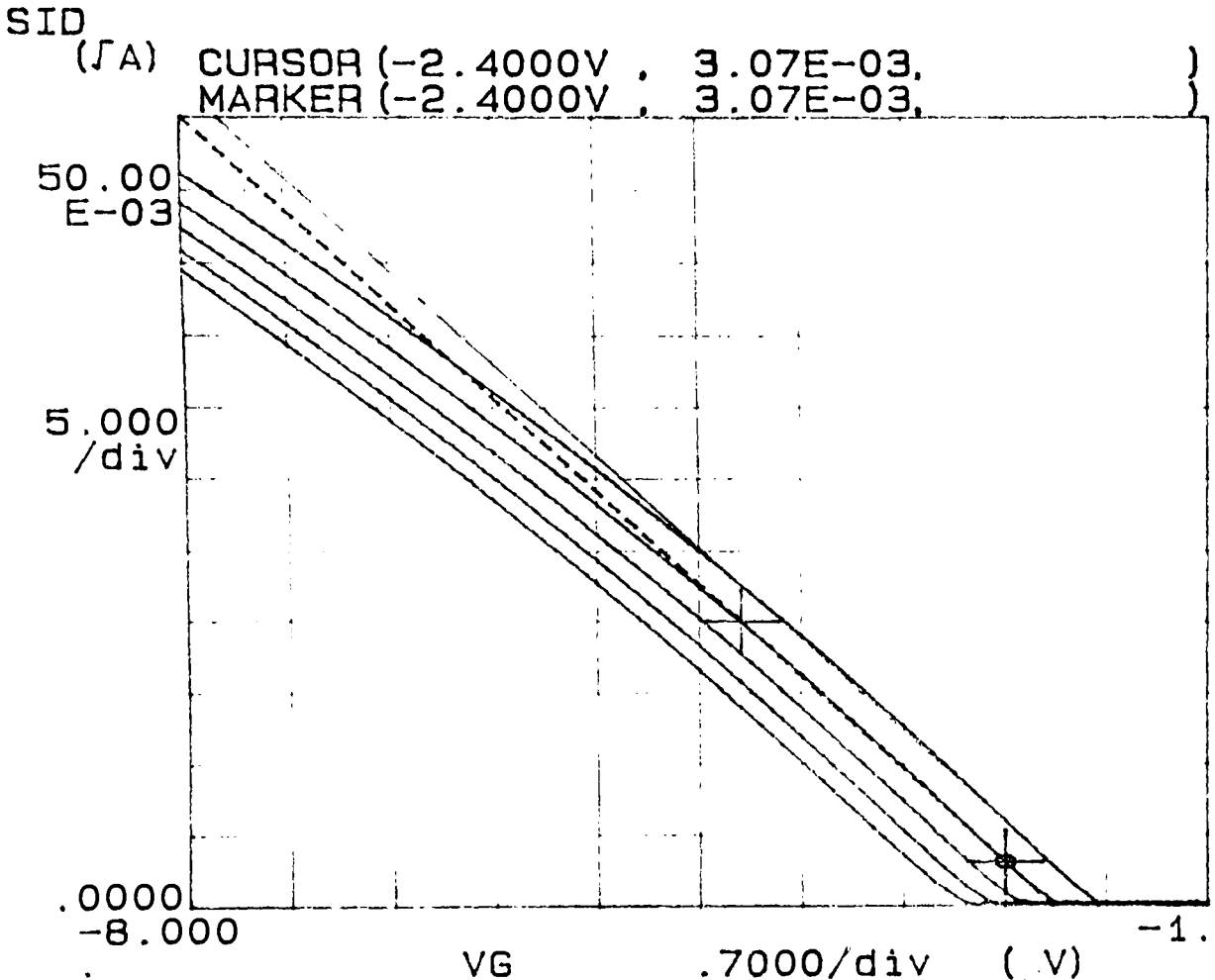
Constants:
VS -Ch1 .0000V
VNW -Ch4 5.0000V

	GRAD	1/GRAD	Xintercept	Yintercept
LINE1	-172E-06	-5.80E+03	-2.04E+00	-351E-06
LINE2				

GM (/Ω) = ΔID/ΔVG

****** GRAPHICS PLOT ******

T4, P-CH ENH, POLY 2, 80X6um



Variable1:
VG -Ch2
Linear sweep
Start -1.0000V
Stop -8.0000V
Step - .0700V

Variable2:
VNW -Ch4
Start 3.0000V
Stop 11.000V
Step 2.0000V

Constants:
VS -Ch1 .0000V
VB -Vs1 .0000V

	GRAD	1/GRAD	Xintercept	Yintercept
LINE1	-9.18E-03	-109E+00	-1.76E+00	-16.1E-03
LINE2	-9.28E-03	-108E+00	-2.07E+00	-19.2E-03

SID (ΓA) = ΓID

```
*******02/09/86 ********  SPICE 2G.5 (10AUG81)  ********17:23:11*****

        IDS VS VDS FOR THE EK PMOS T46 TRANSISTORS

****      INPUT LISTING                          TEMPERATURE =   27.000 DEG C

******************************************************************************


*                  C S BELL
*
VSUB 9 0 DC 4.7
VDS 20 0
VGS1 1 0 DC -2
VGS2 2 0 DC -3
VGS3 3 0 DC -4
VGS4 4 0 DC -5
VGS5 5 0 DC -6
M1 11 1 0 9 T46 L=6U W=80U NRS=.1 NRD=.1 AD=1280P AS=1280P PD=192U
+PS=192U
M2 12 2 0 9 T46 L=6U W=80U NRS=.1 NRD=.1 AD=1280P AS=1280P PD=192U
+PS=192U
M3 13 3 0 9 T46 L=6U W=80U NRS=.1 NRD=.1 AD=1280P AS=1280P PD=192U
+PS=192U
M4 14 4 0 9 T46 L=6U W=80U NRS=.1 NRD=.1 AD=1280P AS=1280P PD=192U
+PS=192U
M5 15 5 0 9 T46 L=6U W=80U NRS=.1 NRD=.1 AD=1280P AS=1280P PD=192U
+PS=192U
VID1 20 11 0
VID2 20 12 0
VID3 20 13 0
VID4 20 14 0
VID5 20 15 0

 .MODEL T26 NMOS LAMBDA=.01750 UO=610 TPG=1 TOX=.0711U
+XJ=.5U NSUB=4.008E14 RSH=48.92 PB=.871 CGSO=2.91E-10
+CGDO=2.91E-10 CJ=1.77E-4 MJ=.5 CJSW=8.85E-11 MJSW=.3
+LD=.2U LEVEL=2 VTO=.53 GAMMA=.2232 NSS=4.758E11

 .MODEL T280 NMOS LAMBDA=.00155 UO=610 TPG=1 TOX=.0711U
+XJ=.5U NSUB=4.008E14 RSH=48.92 PB=.871 CGSO=2.91E-10
+CGDO=2.91E-10 CJ=1.77E-4 MJ=.5 CJSW=8.85E-11 MJSW=.3
+LD=.2U LEVEL=2 VTO=.604 GAMMA=.2509 NSS=4.983E11
+
 .MODEL T46 PMOS LAMBDA=.02750 UO=178 TPG=-1 TOX=.0711U
+XJ=.8U NSUB=3.700E16 RSH=285.6 PB=.719 CGSO=4.85E-10
+CGDO=4.85E-10 CJ=.958E-5 MJ=.5 CJSW=.958E-11 MJSW=.3
+LD=.6U LEVEL=2 VTO=-1.070 GAMMA=.6645 NSS=1.291E11
+
 .MODEL T480 PMOS LAMBDA=.00155 UO=178 TPG=-1 TOX=.0711U
+XJ=.8U NSUB=3.700E16 RSH=285.6 PB=.719 CGSO=4.85E-10
+CGDO=4.85E-10 CJ=.958E-5 MJ=.5 CJSW=.958E-11 MJSW=.3
+LD=.6U LEVEL=2 VTO=-1.009 GAMMA=.7736 NSS=1.478E11
 .WIDTH OUT=80
 .OP
 .DC VDS 0 -7.5 -.183
 .PLOT DC I(VID5) I(VID4) I(VID3) I(VID2) I(VID1)
+(0,-1.43E-3)
 .PRINT DC I(VID5) I(VID4) I(VID3)I(VID2)
 .END
```

IDS VS VDS FOR THE EK PMOS T46 TRANSISTORS

**** MOSFET MODEL PARAMETERS TEMPERATURE = 27.000 DEG C

****

	T26	T280	T46	T480
TYPE	NMOS	NMOS	PMOS	PMOS
LEVEL	2.000	2.000	2.000	2.000
VTO	0.530	0.604	-1.070	-1.009
KP	2.96D-05	2.96D-05	8.65D-06	8.65D-06
GAMMA	0.223	0.251	0.665	0.774
PHI	0.529	0.529	0.763	0.763
LAMBDA	1.75D-02	1.55D-03	2.75D-02	1.55D-03
PB	0.871	0.871	0.719	0.719
CGSO	2.91D-10	2.91D-10	4.85D-10	4.85D-10
CGDO	2.91D-10	2.91D-10	4.85D-10	4.85D-10
RSH	48.920	48.920	285.600	285.600
CJ	1.77D-04	1.77D-04	9.58D-06	9.58D-06
MJ	0.500	0.500	0.500	0.500
CJSW	8.85D-11	8.85D-11	9.58D-12	9.58D-12
MJSW	0.300	0.300	0.300	0.300
TOX	7.11D-08	7.11D-08	7.11D-08	7.11D-08
NSUB	4.01D+14	4.01D+14	3.70D+16	3.70D+16
NSS	4.76D+11	4.98D+11	1.29D+11	1.48D+11
TPG	1.000	1.000	-1.000	-1.000
XJ	5.00D-07	5.00D-07	8.00D-07	8.00D-07
LD	2.00D-07	2.00D-07	6.00D-07	6.00D-07
UO	610.000	610.000	178.000	178.000

IDS VS VDS FOR THE EK PMOS T46 TRANSISTORS

**** DC TRANSFER CURVES TEMPERATURE = 27.000 DEG C

****

VDS	I(VID5)	I(VID4)	I(VID3)	I(VID2)
0.000D+00	-6.517D-12	-6.517D-12	-6.517D-12	-6.268D-12
-1.830D-01	-1.019D-04	-7.682D-05	-5.137D-05	-2.551D-05
-3.660D-01	-1.996D-04	-1.492D-04	-9.796D-05	-4.589D-05
-5.490D-01	-2.931D-04	-2.170D-04	-1.397D-04	-6.107D-05
-7.320D-01	-3.823D-04	-2.802D-04	-1.765D-04	-7.096D-05
-9.150D-01	-4.672D-04	-3.388D-04	-2.083D-04	-7.548D-05
-1.098D+00	-5.477D-04	-3.927D-04	-2.350D-04	-7.614D-05
-1.281D+00	-6.237D-04	-4.417D-04	-2.565D-04	-7.664D-05
-1.464D+00	-6.952D-04	-4.858D-04	-2.728D-04	-7.715D-05
-1.647D+00	-7.621D-04	-5.250D-04	-2.837D-04	-7.765D-05
-1.830D+00	-8.243D-04	-5.591D-04	-2.892D-04	-7.817D-05
-2.013D+00	-8.818D-04	-5.881D-04	-2.910D-04	-7.868D-05
-2.196D+00	-9.344D-04	-6.119D-04	-2.928D-04	-7.921D-05
-2.379D+00	-9.822D-04	-6.304D-04	-2.945D-04	-7.973D-05
-2.562D+00	-1.025D-03	-6.435D-04	-2.963D-04	-8.026D-05
-2.745D+00	-1.063D-03	-6.511D-04	-2.981D-04	-8.079D-05
-2.928D+00	-1.095D-03	-6.550D-04	-2.999D-04	-8.133D-05
-3.111D+00	-1.122D-03	-6.588D-04	-3.017D-04	-8.187D-05
-3.294D+00	-1.144D-03	-6.627D-04	-3.036D-04	-8.242D-05
-3.477D+00	-1.161D-03	-6.666D-04	-3.054D-04	-8.297D-05
-3.660D+00	-1.172D-03	-6.706D-04	-3.073D-04	-8.353D-05
-3.843D+00	-1.179D-03	-6.746D-04	-3.092D-04	-8.409D-05
-4.026D+00	-1.186D-03	-6.786D-04	-3.111D-04	-8.466D-05
-4.209D+00	-1.193D-03	-6.827D-04	-3.131D-04	-8.523D-05
-4.392D+00	-1.200D-03	-6.868D-04	-3.150D-04	-8.581D-05
-4.575D+00	-1.207D-03	-6.910D-04	-3.170D-04	-8.639D-05
-4.758D+00	-1.214D-03	-6.952D-04	-3.190D-04	-8.698D-05
-4.941D+00	-1.221D-03	-6.995D-04	-3.210D-04	-8.758D-05
-5.124D+00	-1.229D-03	-7.038D-04	-3.230D-04	-8.818D-05
-5.307D+00	-1.236D-03	-7.081D-04	-3.251D-04	-8.879D-05
-5.490D+00	-1.244D-03	-7.125D-04	-3.272D-04	-8.940D-05
-5.673D+00	-1.251D-03	-7.170D-04	-3.293D-04	-9.002D-05
-5.856D+00	-1.259D-03	-7.215D-04	-3.314D-04	-9.064D-05
-6.039D+00	-1.267D-03	-7.260D-04	-3.336D-04	-9.128D-05
-6.222D+00	-1.275D-03	-7.306D-04	-3.358D-04	-9.192D-05
-6.405D+00	-1.282D-03	-7.352D-04	-3.380D-04	-9.256D-05
-6.588D+00	-1.291D-03	-7.399D-04	-3.402D-04	-9.322D-05
-6.771D+00	-1.299D-03	-7.447D-04	-3.424D-04	-9.388D-05
-6.954D+00	-1.307D-03	-7.495D-04	-3.447D-04	-9.454D-05
-7.137D+00	-1.315D-03	-7.544D-04	-3.470D-04	-9.522D-05
-7.320D+00	-1.324D-03	-7.593D-04	-3.493D-04	-9.590D-05
-7.503D+00	-1.332D-03	-7.643D-04	-3.517D-04	-9.659D-05

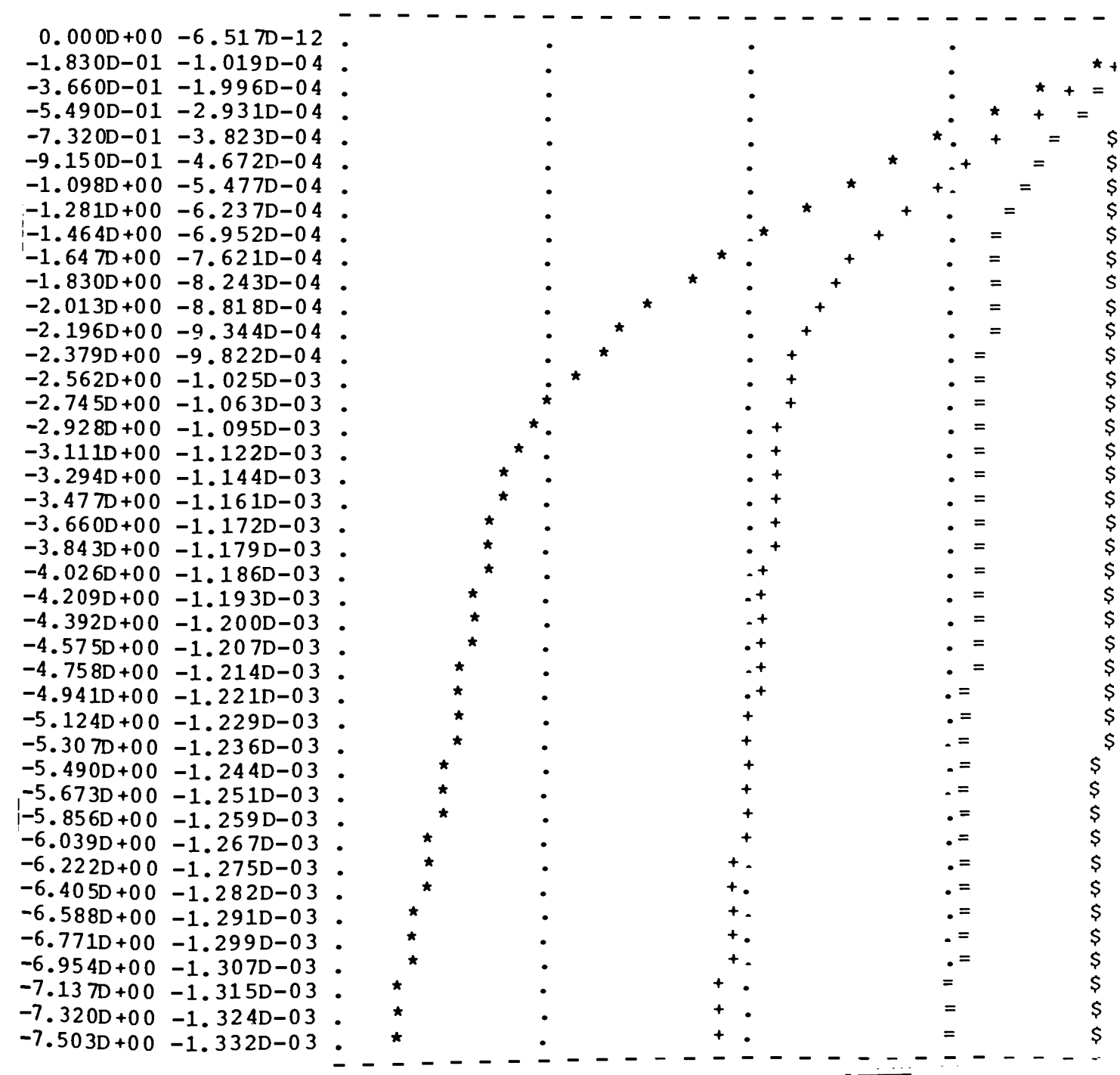
IDS VS VDS FOR THE EK PMOS T46 TRANSISTORS

**** DC TRANSFER CURVES TEMPERATURE = 27.000 DEG C

****

LEGEND:

*: I(VID5)
+: I(VID4)
=: I(VID3)
$: I(VID2)
0: I(VID1)



IDS VS VDS FOR THE EK PMOS T46 TRANSISTORS

**** OPERATING POINT INFORMATION TEMPERATURE = 27.000 DEG C

****

**** MOSFETS

	M1	M2	M3	M4	M5
MODEL	T46	T46	T46	T46	T46
ID	-1.82D-12	-1.82D-12	-1.82D-12	-1.82D-12	-1.82D-12
VGS	-2.000	-3.000	-4.000	-5.000	-6.000
VDS	0.000	0.000	0.000	0.000	0.000
VBS	4.700	4.700	4.700	4.700	4.700
VTH	-1.927	-1.927	-1.927	-1.927	-1.927
VDSAT	-0.064	-0.953	-1.848	-2.748	-3.653
GM	0.00D+00	0.00D+00	0.00D+00	0.00D+00	0.00D+00
GDS	1.05D-05	1.55D-04	2.99D-04	4.43D-04	5.87D-04
GMB	0.00D+00	0.00D+00	0.00D+00	0.00D+00	0.00D+00
CBD	5.47D-15	5.47D-15	5.47D-15	5.47D-15	5.47D-15
CBS	5.47D-15	5.47D-15	5.47D-15	5.47D-15	5.47D-15
CGSOVL	3.88D-14	3.88D-14	3.88D-14	3.88D-14	3.88D-14
CGDOVL	3.88D-14	3.88D-14	3.88D-14	3.88D-14	3.88D-14
CGBOVL	0.00D+00	0.00D+00	0.00D+00	0.00D+00	0.00D+00
CGS	1.24D-13	1.22D-13	1.18D-13	1.15D-13	6.42D-14
CGD	3.30D-15	3.33D-14	4.87D-14	5.80D-14	1.13D-13
CGB	0.00D+00	0.00D+00	0.00D+00	0.00D+00	0.00D+00

JOB CONCLUDED

TOTAL JOB TIME 0.20

T4 p-channel 80u x 80u

Wafer D83-16 Location	I-V i @4.5v uA	Vto	gm gm(max1) u/Ohms	@V	V @25uA	Body Effect Vt Vsub=3	V2 Vsub=5	V3 Vsub=7
23 23	-56.53	-2.16	9.12	-3.64	-4.985	-1.82	-2.16	-2.45
25 23	-53.41	-2.20	8.88	-3.80	-5.088	-1.88	-2.23	-2.52
27 23	-49.19	-2.29	8.51	-3.88	-5.239	-1.88	-2.27	-2.57
26 24	-50.30	-2.27	8.61	-3.96	-5.199	-1.87	-2.24	-2.56
24 24	-54.72	-2.19	8.97	-3.72	-5.045	-1.82	-2.16	-2.47
23 25	-55.70	-2.17	9.04	-3.80	-5.011	-1.80	-2.15	-2.44
25 25	-54.47	-2.20	9.03	-3.80	-5.053	-1.88	-2.24	-2.55
27 25	-49.76	-2.28	8.58	-3.72	-5.218	-1.95	-2.34	-2.64
26 26	-51.35	-2.23	8.62	-3.64	-5.158	-1.92	-2.30	-2.61
24 26	-46.99	-2.31	8.28	-4.04	-5.319	-1.87	-2.23	-2.51
Avg	-52.242	-2.230	8.76	-3.80	-5.132	-1.87	-2.23	-2.53
Std Dev	3.007	0.051	0.266	0.124	0.105	0.044	0.059	0.063
Dev %	5.76	2.29	3.03	3.26	2.05	2.34	2.65	2.50
Var	9.044	0.003	0.071	0.015	0.011	0.002	0.003	0.004

From regression analysis:

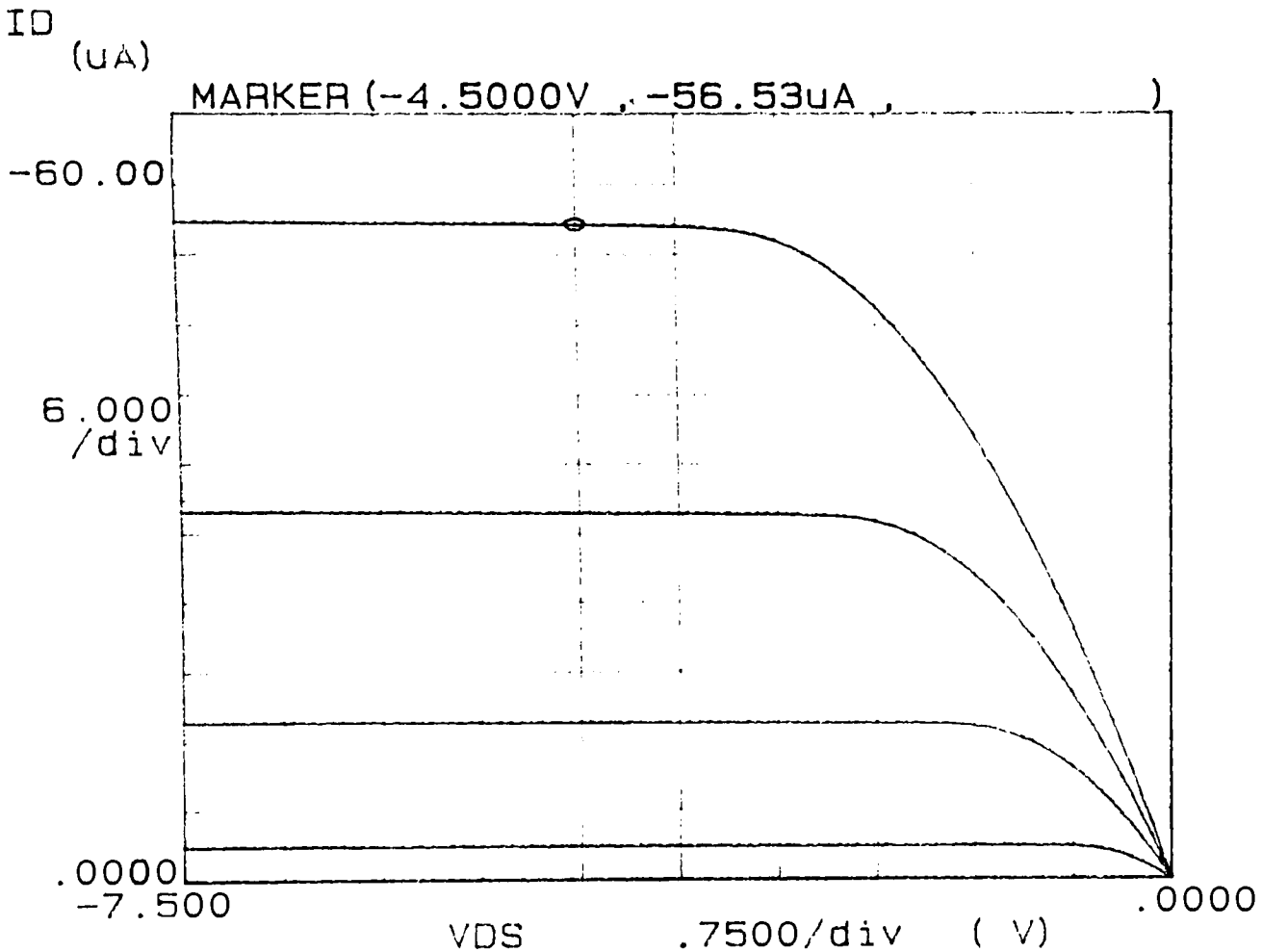
Gamma	Vto	Corr. fit
-0.77364	-1.009	0.959

Other parameters:

Phi f	0.314388
Nsub	3.7E+15
up	210

****** GRAPHICS PLOT ******

T4, P-CH ENH, POLY 2, 80X80um



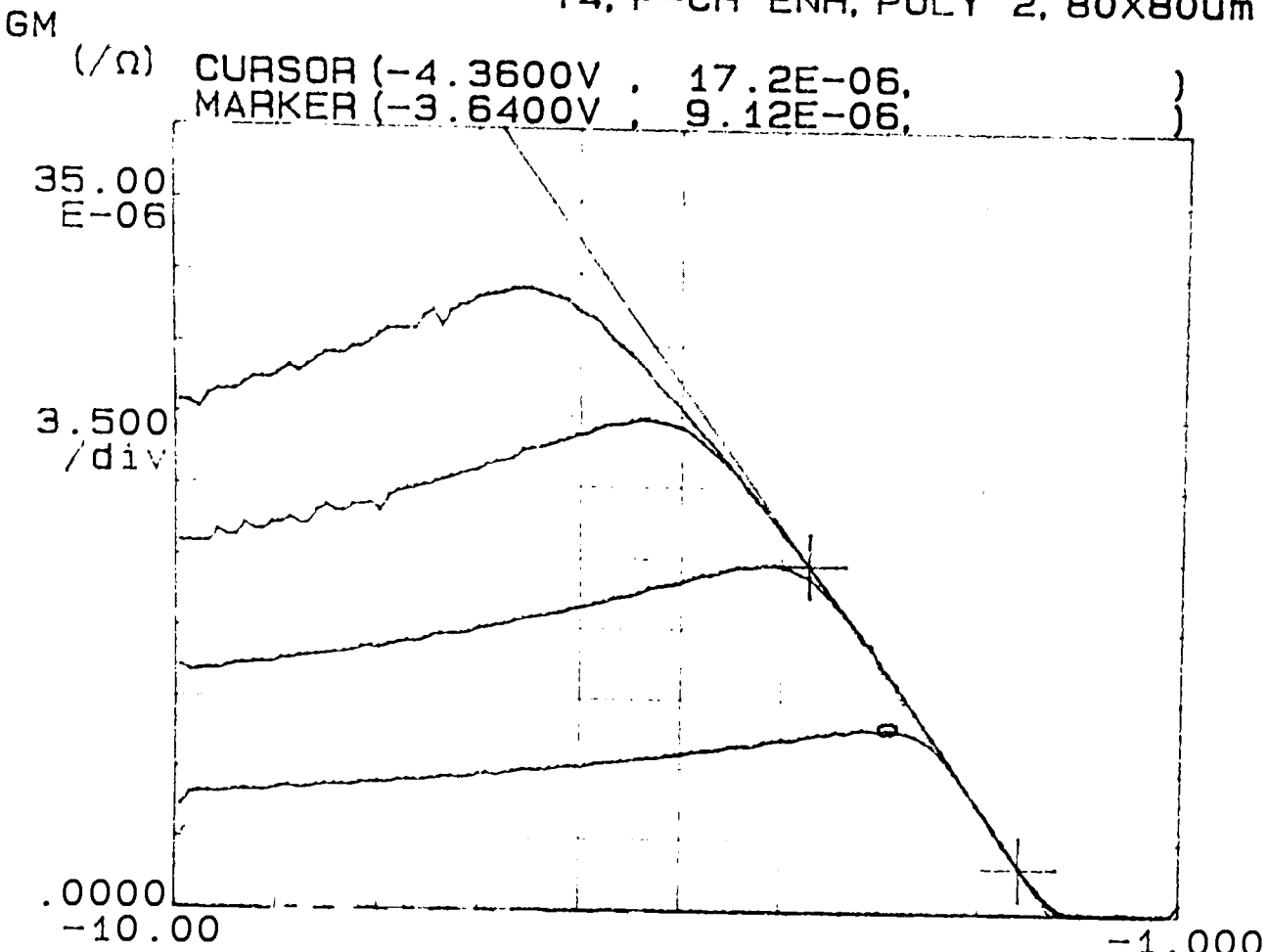
Variable1:
VDS -Ch3
Linear sweep
Start .0000V
Stop -7.5000V
Step - .0750V

Variable2:
VG -Ch2
Start -2.0000V
Stop -6.0000V
Step -1.0000V

Constants:
VS -Ch1 .0000V
VNW -Ch4 5.0000V

****** GRAPHICS PLOT ******

T4, P-CH ENH, POLY 2, 80X80um



	GRAD	1/GRAD	Xintercept	Yintercept
LINE1	-7.81E-06	-128E+03	-2.16E+00	-16.8E-06
LINE2				

GM (/Ω) = ΔID/ΔVG

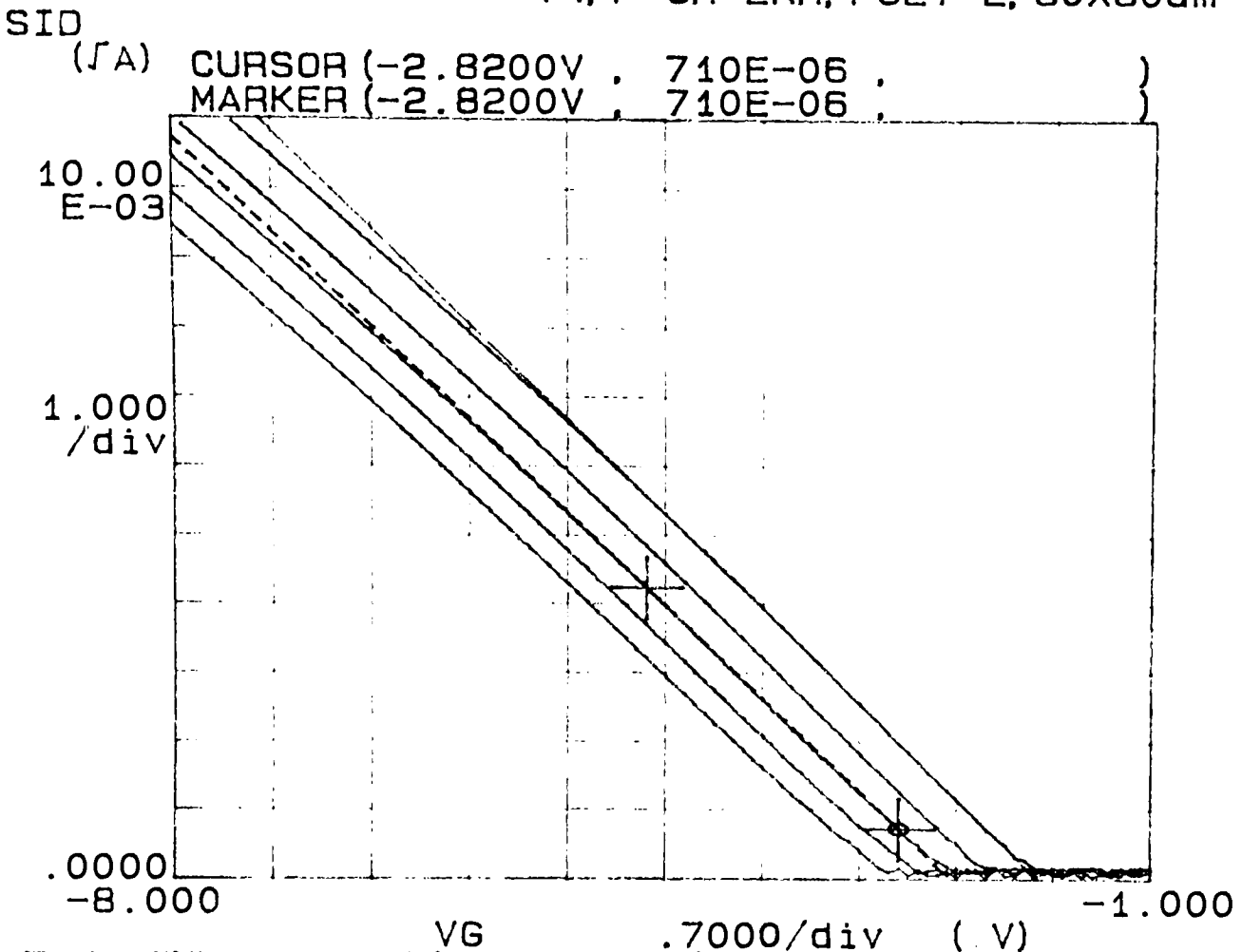
Variable1:
VG -Ch2
Linear sweep
Start -1.0000V
Stop -10.000V
Step - .0800V

Variable2:
VD -Ch3
Start .0000V
Stop -4.0000V
Step -1.0000V

Constants:
VS -Ch1 .0000V
VNW -Ch4 5.0000V

****** GRAPHICS PLOT ******

T4, P-CH ENH, POLY 2, 80X80um



Variable1:
VG -Ch2
Linear sweep
Start -1.0000V
Stop -8.0000V
Step - .0700V

Variable2:
VNW -Ch4
Start 3.0000V
Stop 11.000V
Step 2.0000V

Constants:
VS -Ch1 .0000V
VB -Vs1 .0000V

	GRAD	1/GRAD	Xintercept	Yintercept
LINE1	-1.97E-03	-507E+00	-1.82E+00	-3.59E-03
LINE2	-1.93E-03	-518E+00	-2.45E+00	-4.74E-03

SID (ΓA) = ΓID

```
*******02/09/86 ********  SPICE 2G.5 (10AUG81)  ********17:16:33*****

        IDS VS VDS FOR THE EK PMOS T480 TRANSISTORS

****    INPUT LISTINC                          TEMPERATURE =   27.000 DEG C

**********************************************************************


*                C S BELL
*
VSUB 9 0 DC 4.7
VDS 20 0
VGS1 1 0 DC -2
VGS2 2 0 DC -3
VGS3 3 0 DC -4
VGS4 4 0 DC -5
VGS5 5 0 DC -6
M1 11 1 0 9 T480 L=80U W=80U NRS=.1 NRD=.1 AD=1280P AS=1280P PD=192U
+PS=192U
M2 12 2 0 9 T480 L=80U W=80U NRS=.1 NRD=.1 AD=1280P AS=1280P PD=192U
+PS=192U
M3 13 3 0 9 T480 L=80U W=80U NRS=.1 NRD=.1 AD=1280P AS=1280P PD=192U
+PS=192U
M4 14 4 0 9 T480 L=80U W=80U NRS=.1 NRD=.1 AD=1280P AS=1280P PD=192U
+PS=192U
M5 15 5 0 9 T480 L=80U W=80U NRS=.1 NRD=.1 AD=1280P AS=1280P PD=192U
+PS=192U
VID1 20 11 0
VID2 20 12 0
VID3 20 13 0
VID4 20 14 0
VID5 20 15 0

 .MODEL T26 NMOS LAMBDA=.01750 UO=610 TPG=1 TOX=.0711U
+XJ=.5U NSUB=4.008E14 RSH=48.92 PB=.871 CGSO=2.91E-10
+CGDO=2.91E-10 CJ=1.77E-4 MJ=.5 CJSW=8.85E-11 MJSW=.3
+LD=.2U LEVEL=2 VTO=.53 GAMMA=.2232 NSS=4.758E11

 .MODEL T280 NMOS LAMBDA=.00155 UO=610 TPG=1 TOX=.0711U
+XJ=.5U NSUB=4.008E14 RSH=48.92 PB=.871 CGSO=2.91E-10
+CGDO=2.91E-10 CJ=1.77E-4 MJ=.5 CJSW=8.85E-11 MJSW=.3
+LD=.2U LEVEL=2 VTO=.604 GAMMA=.2509 NSS=4.983E11
+
 .MODEL T46 PMOS LAMBDA=.02000 UO=187 TPG=-1 TOX=.0711U
+XJ=.8U NSUB=3.700E16 RSH=285.6 PB=.719 CGSO=4.85E-10
+CGDO=4.85E-10 CJ=.958E-5 MJ=.5 CJSW=.958E-11 MJSW=.3
+LD=.6U LEVEL=2 VTO=-1.070 GAMMA=.6645 NSS=1.291E11
+
 .MODEL T480 PMOS LAMBDA=.00155 UO=178 TPG=-1 TOX=.0711U
+XJ=.8U NSUB=3.700E16 RSH=285.6 PB=.719 CGSO=4.85E-10
+CGDO=4.85E-10 CJ=.958E-5 MJ=.5 CJSW=.958E-11 MJSW=.3
+LD=.6U LEVEL=2 VTO=-1.009 GAMMA=.7736 NSS=1.478E11
 .WIDTH OUT=80
 .OP
 .DC VDS 0 -7.5 -.183
 .PLOT DC I(VID5) I(VID4) I(VID3) I(VID2) I(VID1)
+(0,-66E-06)
 .PRINT DC I(VID5) I(VID4) I(VID3) I(VID2)
 .END
```

IDS. VS VDS FOR THE EK PMOS T480 TRANSISTORS

**** MOSFET MODEL PARAMETERS TEMPERATURE = 27.000 DEG C

****

	T26	T280	T46	T480
TYPE	NMOS	NMOS	PMOS	PMOS
LEVEL	2.000	2.000	2.000	2.000
VTO	0.530	0.604	-1.070	-1.009
KP	2.96D-05	2.96D-05	9.08D-06	8.65D-06
GAMMA	0.223	0.251	0.665	0.774
PHI	0.529	0.529	0.763	0.763
LAMBDA	1.75D-02	1.55D-03	2.00D-02	1.55D-03
PB	0.871	0.871	0.719	0.719
CGSO	2.91D-10	2.91D-10	4.85D-10	4.85D-10
CGDO	2.91D-10	2.91D-10	4.85D-10	4.85D-10
RSH	48.920	48.920	285.600	285.600
CJ	1.77D-04	1.77D-04	9.58D-06	9.58D-06
MJ	0.500	0.500	0.500	0.500
CJSW	8.85D-11	8.85D-11	9.58D-12	9.58D-12
MJSW	0.300	0.300	0.300	0.300
TOX	7.11D-08	7.11D-08	7.11D-08	7.11D-08
NSUB	4.01D+14	4.01D+14	3.70D+16	3.70D+16
NSS	4.76D+11	4.98D+11	1.29D+11	1.48D+11
TPG	1.000	1.000	-1.000	-1.000
XJ	5.00D-07	5.00D-07	8.00D-07	8.00D-07
LD	2.00D-07	2.00D-07	6.00D-07	6.00D-07
UO	610.000	610.000	187.000	178.000

IDS VS VDS FOR THE EK PMOS T480 TRANSISTORS

**** DC TRANSFER CURVES TEMPERATURE = 27.000 DEG C

****

VDS	I(VID5)	I(VID4)	I(VID3)	I(VID2)
0.000D+00	-6.517D-12	-6.517D-12	-6.517D-12	-6.517D-12
-1.830D-01	-6.030D-06	-4.429D-06	-2.826D-06	-1.221D-06
-3.660D-01	-1.172D-05	-8.519D-06	-5.312D-06	-2.102D-06
-5.490D-01	-1.708D-05	-1.227D-05	-7.459D-06	-2.642D-06
-7.320D-01	-2.210D-05	-1.569D-05	-9.268D-06	-2.843D-06
-9.150D-01	-2.679D-05	-1.877D-05	-1.074D-05	-2.845D-06
-1.098D+00	-3.113D-05	-2.151D-05	-1.187D-05	-2.846D-06
-1.281D+00	-3.515D-05	-2.391D-05	-1.267D-05	-2.847D-06
-1.464D+00	-3.883D-05	-2.598D-05	-1.312D-05	-2.848D-06
-1.647D+00	-4.217D-05	-2.772D-05	-1.325D-05	-2.850D-06
-1.830D+00	-4.518D-05	-2.911D-05	-1.325D-05	-2.851D-06
-2.013D+00	-4.786D-05	-3.018D-05	-1.326D-05	-2.852D-06
-2.196D+00	-5.020D-05	-3.090D-05	-1.326D-05	-2.853D-06
-2.379D+00	-5.221D-05	-3.129D-05	-1.327D-05	-2.854D-06
-2.562D+00	-5.388D-05	-3.137D-05	-1.327D-05	-2.855D-06
-2.745D+00	-5.522D-05	-3.138D-05	-1.328D-05	-2.856D-06
-2.928D+00	-5.623D-05	-3.139D-05	-1.328D-05	-2.857D-06
-3.111D+00	-5.691D-05	-3.140D-05	-1.328D-05	-2.859D-06
-3.294D+00	-5.725D-05	-3.141D-05	-1.329D-05	-2.860D-06
-3.477D+00	-5.730D-05	-3.142D-05	-1.329D-05	-2.861D-06
-3.660D+00	-5.732D-05	-3.143D-05	-1.330D-05	-2.862D-06
-3.843D+00	-5.734D-05	-3.144D-05	-1.330D-05	-2.863D-06
-4.026D+00	-5.735D-05	-3.145D-05	-1.331D-05	-2.864D-06
-4.209D+00	-5.737D-05	-3.146D-05	-1.331D-05	-2.865D-06
-4.392D+00	-5.739D-05	-3.147D-05	-1.332D-05	-2.866D-06
-4.575D+00	-5.741D-05	-3.148D-05	-1.332D-05	-2.867D-06
-4.758D+00	-5.742D-05	-3.149D-05	-1.332D-05	-2.868D-06
-4.941D+00	-5.744D-05	-3.150D-05	-1.333D-05	-2.870D-06
-5.124D+00	-5.746D-05	-3.151D-05	-1.333D-05	-2.871D-06
-5.307D+00	-5.748D-05	-3.152D-05	-1.334D-05	-2.872D-06
-5.490D+00	-5.750D-05	-3.153D-05	-1.334D-05	-2.873D-06
-5.673D+00	-5.751D-05	-3.154D-05	-1.335D-05	-2.874D-06
-5.856D+00	-5.753D-05	-3.155D-05	-1.335D-05	-2.875D-06
-6.039D+00	-5.755D-05	-3.156D-05	-1.335D-05	-2.876D-06
-6.222D+00	-5.757D-05	-3.157D-05	-1.336D-05	-2.877D-06
-6.405D+00	-5.758D-05	-3.158D-05	-1.336D-05	-2.878D-06
-6.588D+00	-5.760D-05	-3.159D-05	-1.337D-05	-2.879D-06
-6.771D+00	-5.762D-05	-3.160D-05	-1.337D-05	-2.880D-06
-6.954D+00	-5.764D-05	-3.161D-05	-1.338D-05	-2.881D-06
-7.137D+00	-5.765D-05	-3.162D-05	-1.338D-05	-2.882D-06
-7.320D+00	-5.767D-05	-3.163D-05	-1.339D-05	-2.883D-06
-7.503D+00	-5.769D-05	-3.164D-05	-1.339D-05	-2.885D-06

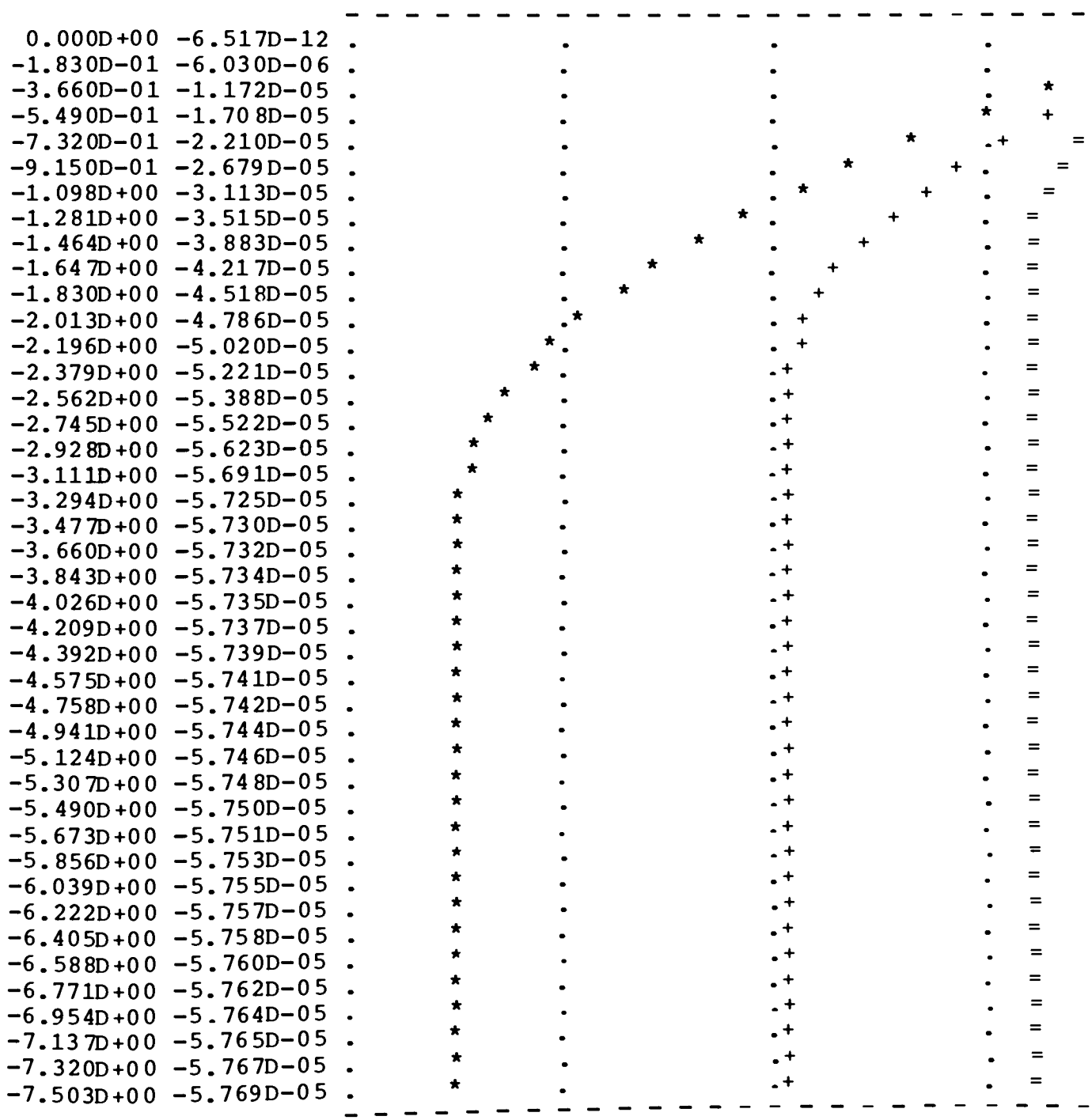
IDS VS VDS FOR THE EK PMOS T480 TRANSISTORS

**** DC TRANSFER CURVES TEMPERATURE = 27.000 DEG C

****

LEGEND:

*: I(VID5)
+: I(VID4)
=: I(VID3)
$: I(VID2)
0: I(VID1)



IDS VS VDS FOR THE EK PMOS T480 TRANSISTORS

**** OPERATING POINT INFORMATION TEMPERATURE = 27.000 DEG C

****

**** MOSFETS

	M1	M2	M3	M4	M5
MODEL	T480	T480	T480	T480	T480
ID	-1.82D-12	-1.82D-12	-1.82D-12	-1.82D-12	-1.82D-12
VGS	-2.000	-3.000	-4.000	-5.000	-6.000
VDS	0.000	0.000	0.000	0.000	0.000
VBS	4.700	4.700	4.700	4.700	4.700
VTH	-2.133	-2.133	-2.133	-2.133	-2.133
VDSAT	0.000	-0.748	-1.618	-2.494	-3.377
GM	0.00D+00	0.00D+00	0.00D+00	0.00D+00	0.00D+00
GDS	0.00D+00	7.61D-06	1.64D-05	2.52D-05	3.39D-05
GMB	0.00D+00	0.00D+00	0.00D+00	0.00D+00	0.00D+00
CBD	5.47D-15	5.47D-15	5.47D-15	5.47D-15	5.47D-15
CBS	5.47D-15	5.47D-15	5.47D-15	5.47D-15	5.47D-15
CGSOVL	3.88D-14	3.88D-14	3.88D-14	3.88D-14	3.88D-14
CGDOVL	3.88D-14	3.88D-14	3.88D-14	3.88D-14	3.88D-14
CGBOVL	0.00D+00	0.00D+00	0.00D+00	0.00D+00	0.00D+00
CCS	1.33D-12	2.01D-12	1.96D-12	1.91D-12	1.86D-12
CGD	-3.94D-30	4.63D-13	7.47D-13	9.16D-13	1.03D-12
CGB	5.34D-13	0.00D+00	0.00D+00	0.00D+00	0.00D+00

JOB CONCLUDED

TOTAL JOB TIME 0.19

APPENDIX C

PARAMETER EXTRACTION CALCULATIONS

This appendix contains the worksheets used to calculate N_{ss}, N_{sub}, V_T, and γ, the body effect parameter. For the techniquess applied in these calculations, refer to pages 24-28 in the report. These worksheets are generated by a software package, Formula One, for the IBM PC. Formula One is a general purpose spreadsheet program that offers iterative equation solving, curve fitting, and regression analysis. It is list-oriented, and data can be transferred to or from Lotus 123 spreadsheets. Formula One is supported by Alloy Computer Products, Inc., 100 Pennsylvania Avenue, Framingham, MA 01701.

Body Effect n-channel 80u x 6u

Vt measured	@Vsub	Vt gamma ← Regression results
.524	0	.53027
.530	0	-.22324
.554	0	
.536	0	
.528	0	
.517	0	
.522	0	
.586	0	
.527	0	
.531	0	
.912	-2	
.927	-2	
.943	-2	
.942	-2	
.911	-2	
.893	-2	
.953	-2	
1.010	-2	
.995	-2	
.932	-2	
1.070	-4	
1.110	-4	
1.140	-4	
1.120	-4	
1.080	-4	
1.060	-4	
1.140	-4	
1.210	-4	
1.190	-4	
1.110	-4	

Regression Analysis Sheet

Dependent Variable:	Vmsn6
Coefficient List:	gamma
Correlation Coefficient:	.9759006991
Intercept:	.530274607 V_t

Independent Variable	Corresponding Coefficient
Vsubstrate	-.22324124 γ

Equation Sheet

St	Equation
*	Oms=Om-(Chi+Eg/2-Phi_f)
*	Eox=Erx*E0
*	Cox=Eox/tox
*	Vt=Oms-q*Nss/Cox-2*Phi_f-2/Cox*(q*Esi*E0*Nsub*Phi_f)^.5
*	NSUB=1/(q*un*rho)
*	Phi_f=kb*ln(Nsub/ni)
*	Vtp=(Vsub+2*Phi_f)
*	Sn=sign(Vtp)
*	Cp=(2*Phi_f)^.5
*	Vsubstrate=Sn*(Sn*Vtp)^.5-Cp

Variable Sheet

St	Name	Value	Dsp Unit	Cal Unit	Comments
O	Phi_f	.2583515081			Fermi potential
I	q	1.602E-19			Electron charge
I	NSUB	4.01E14	atom/cm3	atom/cm3	Calc for comparison
I	ni	1.45E10	1/cm3	1/cm3	intrinsic carrier conc
O	rho	25.51897818	Ohm/sq	Ohm/sq	Sheet resistance
I	kb	.025256	Volt	Volt	kT/q
I	un	610		cm2/Vsec	N-ch mobility, Vds=10,
I	up	210		cm2/Vsec	P-ch mobility, Vds=10,
L	gamma				
OL	Vtp				Vtemp
IL	Vsub				n-channel substrate bi
IL	Vmsn6				measurements
IL	Vmsn80				measurements
IL	Vmsp6				measurements
IL	Vmsp80				measurements
OL	Vsubstrate				calculate prior to reg
IL	Vsub1				p-channel substrate bi
O	Oms	-.3516484918			
I	Om	4.1			
I	Chi	4.15			
I	Eg	1.12			
O	Cox	.0000000485			
O	Eox	3.45306E-13			
I	tox	.00000711	cm		
IL	Vt				threshold voltages
OL	Nss				surface states
I	Nsub	4.017E14	atom/cm3		
OL	Sn				sign
O	Cp	.7188205731			pre-calculation
I	Erx	3.9			Oxide
I	E0	8.854E-14	F/cm		
I	Esi	11.7			Silicon

Body Effect n-channel 80u x80u

Vt measured	Vsub	Vt gamma
.559	0	.60431
.602	0	-.25090
.623	0	
.620	0	
.591	0	
.587	0	
.618	0	
.666	0	
.649	0	
.612	0	
.988	-2	
1.050	-2	
1.070	-2	
1.060	-2	
1.020	-2	
1.010	-2	
1.070	-2	
1.130	-2	
1.110	-2	
1.060	-2	
1.220	-4	
1.270	-4	
1.300	-4	
1.280	-4	
1.230	-4	
1.210	-4	
1.300	-4	
1.360	-4	
1.340	-4	
1.270	-4	

Regression Analysis Sheet

Dependent Variable:	Vmsn80
Coefficient List:	gamma
Correlation Coefficient:	.9720538131
Intercept:	.6043109149 V_t

Independent Variable	Corresponding Coefficient
Vsubstrate	-.2509045842 γ

Equation Sheet

St	Equation
*	Oms=Om-(Chi+Eg/2-Phi_f)
*	Eox=Erx*E0
*	Cox=Eox/tox
*	Vt=Oms-q*Nss/Cox-2*Phi_f-2/Cox*(q*Esi*E0*Nsub*Phi_f)^.5
*	NSUB=1/(q*un*rho)
*	Phi_f=kb*ln(Nsub/ni)
*	Vtp=(Vsub+2*Phi_f)
*	Sn=sign(Vtp)
*	Cp=(2*Phi_f)^.5
*	Vsubstrate=Sn*(Sn*Vtp)^.5-Cp

Variable Sheet

St	Name	Value	Dsp Unit	Cal Unit	Comments
O	Phi_f	.2583515081			Fermi potential
I	q	1.602E-19			Electron charge
I	NSUB	4.01E14	atom/cm3	atom/cm3	Calc for comparison
I	ni	1.45E10	1/cm3	1/cm3	intrinsic carrier conc
O	rho	25.51897818	Ohm/sq	Ohm/sq	Sheet resistance
I	kb	.025256	Volt	Volt	kT/q
I	un	610		cm2/Vsec	N-ch mobility, Vds=10.
I	up	210		cm2/Vsec	P-ch mobility, Vds=10.
L	gamma				
OL	Vtp				Vtemp
IL	Vsub				n-channel substrate bi
IL	Vmsn6				measurements
IL	Vmsn80				measurements
IL	Vmsp6				measurements
IL	Vmsp80				measurements
OL	Vsubstrate				calculate prior to rec
IL	Vsub1				p-channel substrate bi
O	Oms	-.3516484918			
I	Om	4.1			
I	Chi	4.15			
I	Eg	1.12			
O	Cox	.0000000485			
O	Eox	3.45306E-13			
I	tox	.00000711	cm		
IL	Vt				threshold voltages
OL	Nss				surface states
I	Nsub	4.017E14	atom/cm3		
OL	Sn				sign
O	Cp	.7188205731			pre-calculation
I	Erx	3.9			Oxide
I	E0	8.854E-14	F/cm		
I	Esi	11.7			Silicon

Body Effect p-channel 80u x 6u

Vt measured	Vsub	Vt gamma
-1.740	3	-1.07071
-1.800	3	-.66448
-1.840	3	
-1.820	3	
-1.760	3	
-1.740	3	
-1.830	3	
-1.880	3	
-1.840	3	
-1.800	3	
-2.070	5	
-2.120	5	
-2.150	5	
-2.130	5	
-2.060	5	
-2.050	5	
-2.150	5	
-2.220	5	
-2.190	5	
-2.120	5	
-2.220	7	
-2.350	7	
-2.410	7	
-2.390	7	
-2.310	7	
-2.290	7	
-2.410	7	
-2.500	7	
-2.470	7	
-2.380	7	

Regression Analysis Sheet

Dependent Variable:	Vmsp6
Coefficient List:	gamma
Correlation Coefficient:	.9355776657
Intercept:	-1.070705396

Independent Variable	Corresponding Coefficient
Vsubstrate	-.6644818502

Equation Sheet

St	Equation
*	Oms=Om-(Chi+Eg/2-Phi_f)
*	Eox=Erx*E0
*	Cox=Eox/tox
*	Vt=Oms-q*Nss/Cox-2*Phi_f-2/Cox*(q*Esi*E0*Nsub*Phi_f)^.5
*	NSUB=1/(q*up*rho)
*	Phi_f=kb*ln(Nsub/ni)
*	Vtp=(Vsub1+2*Phi_f)
*	Sn=sign(Vtp)
*	Cp=(2*Phi_f)^.5
*	Vsubstrate=Sn*(Sn*Vtp)^.5-Cp

Variable Sheet

St	Name	Value	Dsp Unit	Cal Unit	Comments
U	Phi_f	.3143885011			Fermi potential
I	q	1.602E-19			Electron charge
O	NSUB	7.96483087E12	atom/cm3	atom/cm3	Calc for comparison
I	ni	1.45E10	1/cm3	1/cm3	intrinsic carrier con
I	rho	3732	Ohm/sq	Ohm/sq	Sheet resistance
I	kb	.025256	Volt	Volt	kT/q
I	un	760		cm2/Vsec	N-ch mobility, Vds=1(
I	up	210		cm2/Vsec	P-ch mobility, Vds=1(
L	gamma				
OL	Vtp				Vtemp
IL	Vsub				n-channel substrate b
IL	Vmsn6				measurements
IL	Vmsn80				measurements
IL	Vmsp6				measurements
IL	Vmsp80				measurements
OL	Vsubstrate				calcualte prior to re
IL	Vsub1				p-channel substrate b
O	Oms	-.2956114988			
I	Om	4.1			
I	Chi	4.15			
I	Eg	1.12			
O	Cox	.0000000485			
O	Eox	3.45306E-13			
I	tox	.00000711	cm		
L	Vt				threshold voltages
L	Nss				surface states
I	Nsub	3.694E15	atom/cm3		
OL	Sn				sign
O	Cp	.7929546029			pre-calculation
I	Erx	3.9			Oxide
I	E0	8.854E-14	F/cm		
I	Esi	11.7			Silicon

Body Effect p-channel 80u x80u

Vt measured	Vsub	Vt gamma
-1.820	3	-1.00912
-1.880	3	-.77364
-1.880	3	
-1.870	3	
-1.820	3	
-1.800	3	
-1.880	3	
-1.950	3	
-1.920	3	
-1.870	3	
-2.160	5	
-2.230	5	
-2.270	5	
-2.240	5	
-2.160	5	
-2.150	5	
-2.240	5	
-2.340	5	
-2.300	5	
-2.230	5	
-2.450	7	
-2.520	7	
-2.570	7	
-2.560	7	
-2.470	7	
-2.440	7	
-2.550	7	
-2.640	7	
-2.610	7	
-2.510	7	

Regression Analysis Sheet

Dependent Variable:	Vmsp80
Coefficient List:	gamma
Correlation Coefficient:	.9590938969
Intercept:	-1.009122797

Independent Variable	Corresponding Coefficient
Vsubstrate	-.7736411525

Equation Sheet

St	Equation
*	Oms=Om-(Chi+Eg/2-Phi_f)
*	Eox=Erx*E0
*	Cox=Eox/tox
*	Vt=Oms-q*Nss/Cox-2*Phi_f-2/Cox*(q*Esi*E0*Nsub*Phi_f)^.5
*	NSUB=1/(q*up*rho)
*	Phi_f=kb*ln(Nsub/ni)
*	Vtp=(Vsub1+2*Phi_f)
*	Sn=sign(Vtp)
*	Cp=(2*Phi_f)^.5
*	Vsubstrate=Sn*(Sn*Vtp)^.5-Cp

Variable Sheet

St	Name	Value	Dsp Unit	Cal Unit	Comments
	Phi_f	.3143885011			Fermi potential
I	q	1.602E-19			Electron charge
O	NSUB	7.96483087E12	atom/cm3	atom/cm3	Calc for comparison
I	ni	1.45E10	1/cm3	1/cm3	intrinsic carrier co
I	rho	3732	Ohm/sq	Ohm/sq	Sheet resistance
I	kb	.025256	Volt	Volt	kT/q
I	un	760		cm2/Vsec	N-ch mobility, Vds=1
I	up	210		cm2/Vsec	P-ch mobility, Vds=1
L	gamma				
OL	Vtp				Vtemp
IL	Vsub				n-channel substrate
IL	Vmsn6				measurements
IL	Vmsn80				measurements
IL	Vmsp6				measurements
IL	Vmsp80				measurements
OL	Vsubstrate				calcualte prior to r
IL	Vsub1				p-channel substrate t
O	Oms	-.2956114988			
I	Om	4.1			
I	Chi	4.15			
I	Eg	1.12			
O	Cox	.0000000485			
O	Eox	3.45306E-13			
I	tox	.00000711	cm		
IL	Vt				threshold voltages
	Nss				surface states
	Nsub	3.694E15	atom/cm3		
OL	Sn				sign
O	Cp	.7929546029			pre-calculation
I	Erx	3.9			Oxide
I	E0	8.854E-14	F/cm		
I	Esi	11.7			Silicon

Nsub calculation

gamma	Nsub	
-.22324	3.542E 14	4.008×10^{14}
-.25090	4.474E 14	
-.66448	3.138E 15	3.695×10^{15}
-.77364	4.253E 15	

========== Equation Sheet ==========

St	Equation
*	Eox=E0*Erx
*	Cox=Eox/tox
*	NSUB=gamma^2*Cox^2/(2*q*ESi*E0)

========== Variable Sheet ==========

St	Name	Value	Dsp Unit	Cal Unit	Comments
I	q	1.602E-19			Electron charge
OL	NSUB		atom/cm3	atom/cm3	Substrate doping con
) L	gamma				
U	Cox	.0000000485	F/cm^2		
O	Eox	3.45306E-13			
I	tox	.00000711	cm		
I	ESi	11.7			
I	E0	8.854E-14	F/cm		
I	Erx	3.9			

Calculation of surface states

Vt regressed	Nss calculated	
.530	-4.758E 11	T2 6μ
.604	-4.983E 11	T2 80μ

Calculation of surface states

Vt regressed	Nss calculated	
-1.070	-1.291E 11	T4 6μ
-1.009	-1.478E 11	T4 80μ

Equation Sheet

St	Equation
	Oms=Om-(Chi+Eg/2-Phi_f)
	Eox=Erx*E0
	Cox=Eox/tox
	Vt=Oms-q*Nss/Cox-2*Phi_f-2/Cox*(q*Esi*E0*Nsub*Phi_f)^.5
	NSUB=1/(q*un*rho)
	Phi_f=kb*ln(Nsub/ni)
	Vtp=(Vsub+2*Phi_f)
	Sn=sign(Vtp)
	Cp=(2*Phi_f)^.5
	Vsubstrate=Sn*(Sn*Vtp)^.5-Cp

Variable Sheet

St	Name	Value	Dsp Unit	Cal Unit	Comments
O	Phi_f	.2583515081			Fermi potential
I	q	1.602E-19			Electron charge
O	NSUB	8.21341743E14	atom/cm3	atom/cm3	Calc for comparison
I	ni	1.45E10	1/cm3	1/cm3	intrinsic carrier cor
I	rho	10	Ohm/sq	Ohm/sq	Sheet resistance
I	kb	.025256	Volt	Volt	kT/q
I	un	760		cm2/Vsec	N-ch mobility, Vds=1
I	up	210		cm2/Vsec	P-ch mobility, Vds=1
L	gamma				
OL	Vtp				Vtemp
IL	Vsub				n-channel substrate
IL	Vmsn6				measurements
IL	Vmsn80				measurements
IL	Vmsp6				measurements
IL	Vmsp80				measurements
OL	Vsubstrate				calculate prior to r
IL	Vsub1				p-channel substrate
O	Oms	-.3516484918			
I	Om	4.1			
I	Chi	4.15			
I	Eg	1.12			
O	Cox	.0000000485			
O	Eox	3.45306E-13			
I	tox	.00000711	cm		
IL	Vt				threshold voltages
OL	Nss				surface states
I	Nsub	4.017E14	atom/cm3		
OL	Sn				sign
O	Cp	.7188205731			pre-calculation
I	Erx	3.9			Oxide
I	E0	8.854E-14	F/cm		
I	Esi	11.7			Silicon

Table Sheet

APPENDIX D

GATE CLOCK TIMING SPICE SIMULATIONS

TRANSMISSION GATE WITH EK TRANSISTORS Figure 28

INPUT LISTING TEMPERATURE = 27.000 DEG C

****

```
*            FEEDTHROUGH ANALYSIS
*                C S BELL
*
VNWELL 1 2 DC 0
VSRC 2 0 DC 0
VGN 5 0 PULSE(-1 5 1E-6 1E-12 1E-12 2.9E-6 3.5E-6)
VGP 4 0  DC 1
VID 3 6 DC 0
M1 3 5 2 0 T280 L=80U W=80U NRS=.1 NRD=.1 AD=1280P AS=1280P PD=192U
+                              PS=192U
M2 3 4 2 1 T480 L=80U W=80U NRS=.1 NRD=.1 AD=1280P AS=1280P PD=192U
+                              PS=192U
C1 6 0 50P
R1 6 0 75K
 .MODEL T26 NMOS LAMBDA=.0175 UO=610 TPG=1 TOX=.0711U
+XJ=.5U NSUB=4.008E14 RSH=48.92 PB=.871 CGSO=2.91E-10
+CGDO=2.91E-10 CJ=1.77E-4 MJ=.5 CJSW=8.85E-11 MJSW=.3
+LD=.2U LEVEL=2 VTO=.53 GAMMA=.2232 NSS=4.758E11

 .MODEL T280 NMOS LAMBDA=.00155 UO=610 TPG=1 TOX=.0711U
+XJ=.5U NSUB=4.008E14 RSH=48.92 PB=.871 CGSO=2.91E-10
+CGDO=2.91E-10 CJ=1.77E-4 MJ=.5 CJSW=8.85E-11 MJSW=.3
+LD=.2U LEVEL=2 VTO=.604 GAMMA=.2509 NSS=4.983E11
+
 .MODEL T46 PMOS LAMBDA=.0275 UO=178 TPG=-1 TOX=.0711U
+XJ=.8U NSUB=3.7E16 RSH=285.6 PB=.719 CGSO=4.85E-10
+CGDO=4.85E-10 CJ=.958E-5 MJ=.5 CJSW=.958E-11 MJSW=.3
+LD=.6U LEVEL=2 VTO=-1.070 GAMMA=.6645 NSS=1.291E11
+
 .MODEL T480 PMOS LAMBDA=.00155 UO=178 TPG=-1 TOX=.0711U
+XJ=.8U NSUB=3.7E16 RSH=285.6 PB=.719 CGSO=4.85E-10
+CGDO=4.85E-10 CJ=.958E-5 MJ=.5 CJSW=.958E-11 MJSW=.3
+LD=.6U LEVEL=2 VTO=-1.009 GAMMA=.7736 NSS=1.478E11
 .WIDTH OUT=80
 .OPTION LIMPTS=1E6
 .TRAN 1E-7 3.5E-6
 .PLOT TRAN V(6) V(5)
 .END
```

TRANSMISSION GATE WITH EK TRANSISTORS Figure 28

MOSFET MODEL PARAMETERS TEMPERATURE = 27.000 DEG C

****

	T26	T280	T46	T480
TYPE	NMOS	NMOS	PMOS	PMOS
LEVEL	2.000	2.000	2.000	2.000
VTO	0.530	0.604	-1.070	-1.009
KP	2.96D-05	2.96D-05	8.65D-06	8.65D-06
GAMMA	0.223	0.251	0.665	0.774
PHI	0.529	0.529	0.763	0.763
LAMBDA	1.75D-02	1.55D-03	2.75D-02	1.55D-03
PB	0.871	0.871	0.719	0.719
CGSO	2.91D-10	2.91D-10	4.85D-10	4.85D-10
CGDO	2.91D-10	2.91D-10	4.85D-10	4.85D-10
RSH	48.920	48.920	285.600	285.600
CJ	1.77D-04	1.77D-04	9.58D-06	9.58D-06
MJ	0.500	0.500	0.500	0.500
CJSW	8.85D-11	8.85D-11	9.58D-12	9.58D-12
MJSW	0.300	0.300	0.300	0.300
TOX	7.11D-08	7.11D-08	7.11D-08	7.11D-08
NSUB	4.01D+14	4.01D+14	3.70D+16	3.70D+16
NSS	4.76D+11	4.98D+11	1.29D+11	1.48D+11
TPG	1.000	1.000	-1.000	-1.000
XJ	5.00D-07	5.00D-07	8.00D-07	8.00D-07
LD	2.00D-07	2.00D-07	6.00D-07	6.00D-07
UO	610.000	610.000	178.000	178.000

TRANSMISSION GATE WITH EK TRANSISTORS Figure 28

INITIAL TRANSIENT SOLUTION TEMPERATURE = 27.000 DEG C

****

NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE
(1)	0.0000	(2)	0.0000	(3)	0.0000	(4)	1.0000
(5)	-1.0000	(6)	0.0000				

VOLTAGE SOURCE CURRENTS

NAME	CURRENT
VNWELL	-2.230D-39
VSRC	-1.306D-39
VGN	0.000D+00
VGP	0.000D+00
VID	9.240D-40

TOTAL POWER DISSIPATION 0.00D+00 WATTS

*******06/21/86 ******** SPICE 2G.5 (10AUG81) ********10:29:21*****

TRANSMISSION GATE WITH EK TRANSISTORS Figure 28

OPERATING POINT INFORMATION TEMPERATURE = 27.000 DEG C

****

**** MOSFETS

	M1	M2
MODEL	T280	T480
ID	0.00D+00	0.00D+00
VGS	-1.000	1.000
VDS	0.000	0.000
VBS	0.000	0.000

LEGEND:
*: V(6)
+: V(5)

(*)--------- -5.000D-02 0.000D+00 5.000D-02 1.000D-01 1.500D-01

(+)--------- -2.000D+00 0.000D+00 2.000D+00 4.000D+00 6.000D+00

TIME	V(6)
0.000D+00	6.930D-35
1.000D-07	1.187D-18
2.000D-07	1.354D-18
3.000D-07	1.159D-18
4.000D-07	9.017D-19
5.000D-07	6.547D-19
6.000D-07	4.191D-19
7.000D-07	1.935D-19
8.000D-07	-2.222D-20
9.000D-07	-2.281D-19
1.000D-06	-4.440D-19
1.100D-06	7.084D-02
1.200D-06	5.309D-02
1.300D-06	4.096D-02
1.400D-06	3.120D-02
1.500D-06	2.295D-02
1.600D-06	1.754D-02
1.700D-06	1.393D-02
1.800D-06	1.011D-02
1.900D-06	7.104D-03
2.000D-06	5.995D-03
2.100D-06	4.710D-03
2.200D-06	2.895D-03
2.300D-06	2.340D-03
2.400D-06	2.472D-03
2.500D-06	1.417D-03
2.600D-06	5.619D-04
2.700D-06	1.043D-03
2.800D-06	9.799D-04
2.900D-06	9.052D-05
3.000D-06	2.120D-04
3.100D-06	8.629D-04
3.200D-06	1.960D-04
3.300D-06	-3.571D-04
3.400D-06	3.427D-04
3.500D-06	7.476D-04

JOB CONCLUDED
TOTAL JOB TIME 0.17

TRANSMISSION GATE WITH EK TRANSISTORS Figure 29

INPUT LISTING TEMPERATURE = 27.000 DEG C

****

```
*            FEEDTHROUGH ANALYSIS
*                C S BELL
*
VNWELL 1 2 DC 0
VSRC 2 0 DC 0
VGP 4 0 PULSE(1 -6.5 1E-6 1E-12 1E-12 2.5E-6 3.5E-6)
VGN 5 0  DC 0
VID 3 6 DC 0
M1 3 5 2 0 T280 L=80U W=80U NRS=.1 NRD=.1 AD=1280P AS=1280P PD=192U
+                           PS=192U
M2 3 4 2 1 T480 L=80U W=80U NRS=.1 NRD=.1 AD=1280P AS=1280P PD=192U
+                           PS=192U
C1 6 0 50P
R1 6 0 75K
 .MODEL T26 NMOS LAMBDA=.0175 UO=610 TPG=1 TOX=.0711U
+XJ=.5U NSUB=4.008E14 RSH=48.92 PB=.871 CGSO=2.91E-10
+CGDO=2.91E-10 CJ=1.77E-4 MJ=.5 CJSW=8.85E-11 MJSW=.3
+LD=.2U LEVEL=2 VTO=.53 GAMMA=.2232 NSS=4.758E11

 .MODEL T280 NMOS LAMBDA=.00155 UO=610 TPG=1 TOX=.0711U
+XJ=.5U NSUB=4.008E14 RSH=48.92 PB=.871 CGSO=2.91E-10
+CGDO=2.91E-10 CJ=1.77E-4 MJ=.5 CJSW=8.85E-11 MJSW=.3
+LD=.2U LEVEL=2 VTO=.604 GAMMA=.2509 NSS=4.983E11
+
 .MODEL T46 PMOS LAMBDA=.0275 UO=178 TPG=-1 TOX=.0711U
+XJ=.8U NSUB=3.7E16 RSH=285.6 PB=.719 CGSO=4.85E-10
+CGDO=4.85E-10 CJ=.958E-5 MJ=.5 CJSW=.958E-11 MJSW=.3
+LD=.6U LEVEL=2 VTO=-1.070 GAMMA=.6645 NSS=1.291E11
+
 .MODEL T480 PMOS LAMBDA=.00155 UO=178 TPG=-1 TOX=.0711U
+XJ=.8U NSUB=3.7E16 RSH=285.6 PB=.719 CGSO=4.85E-10
+CGDO=4.85E-10 CJ=.958E-5 MJ=.5 CJSW=.958E-11 MJSW=.3
+LD=.6U LEVEL=2 VTO=-1.009 GAMMA=.7736 NSS=1.478E11
 .WIDTH OUT=80
 .OPTION LIMPTS=1E6
 .TRAN 1E-7 3.5E-6
 .PLOT TRAN V(6) V(4)
 .END
```

TRANSMISSION GATE WITH EK TRANSISTORS Figure 29

MOSFET MODEL PARAMETERS TEMPERATURE = 27.000 DEG C

****

	T26	T280	T46	T480
TYPE	NMOS	NMOS	PMOS	PMOS
LEVEL	2.000	2.000	2.000	2.000
VTO	0.530	0.604	-1.070	-1.009
KP	2.96D-05	2.96D-05	8.65D-06	8.65D-06
GAMMA	0.223	0.251	0.665	0.774
PHI	0.529	0.529	0.763	0.763
LAMBDA	1.75D-02	1.55D-03	2.75D-02	1.55D-03
PB	0.871	0.871	0.719	0.719
CGSO	2.91D-10	2.91D-10	4.85D-10	4.85D-10
CGDO	2.91D-10	2.91D-10	4.85D-10	4.85D-10
RSH	48.920	48.920	285.600	285.600
CJ	1.77D-04	1.77D-04	9.58D-06	9.58D-06
MJ	0.500	0.500	0.500	0.500
CJSW	8.85D-11	8.85D-11	9.58D-12	9.58D-12
MJSW	0.300	0.300	0.300	0.300
TOX	7.11D-08	7.11D-08	7.11D-08	7.11D-08
NSUB	4.01D+14	4.01D+14	3.70D+16	3.70D+16
NSS	4.76D+11	4.98D+11	1.29D+11	1.48D+11
TPG	1.000	1.000	-1.000	-1.000
XJ	5.00D-07	5.00D-07	8.00D-07	8.00D-07
LD	2.00D-07	2.00D-07	6.00D-07	6.00D-07
UO	610.000	610.000	178.000	178.000

*******06/21/86 ******** SPICE 2G.5 (10AUG81) ********10:35:02*****

TRANSMISSION GATE WITH EK TRANSISTORS Figure 29

INITIAL TRANSIENT SOLUTION TEMPERATURE = 27.000 DEG C

****

NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE
(1)	0.0000	(2)	0.0000	(3)	0.0000	(4)	1.0000
(5)	0.0000	(6)	0.0000				

VOLTAGE SOURCE CURRENTS

NAME	CURRENT
VNWELL	-2.230D-39
VSRC	-1.306D-39
VGP	0.000D+00
VGN	0.000D+00
VID	9.240D-40

TOTAL POWER DISSIPATION 0.00D+00 WATTS

*******06/21/86 ******** SPICE 2G.5 (10AUG81) ********10:35:02*****

TRANSMISSION GATE WITH EK TRANSISTORS Figure 29

OPERATING POINT INFORMATION TEMPERATURE = 27.000 DEG C

****

**** MOSFETS

	M1	M2
MODEL	T280	T480
ID	0.00D+00	0.00D+00
VGS	0.000	1.000
VDS	0.000	0.000
VBS	0.000	0.000

TRANSMISSION GATE WITH EK TRANSISTORS Figure 29

TRANSIENT ANALYSIS TEMPERATURE = 27.000 DEG C

****

LEGEND:
*: V(6)
+: V(4)

```
(*)--------- -1.500D-01     -1.000D-01     -5.000D-02      0.000D+00   5.000D-02
(+)--------- -1.000D+01     -5.000D+00      0.000D+00      5.000D+00   1.000D+01
  TIME       V(6)
0.000D+00   6.930D-35 .                .              .   +          *
1.000D-07  -4.623D-29 .                .              .   +          *
2.000D-07  -5.265D-29 .                .              .   +          *
3.000D-07  -5.771D-29 .                .              .   +          *
4.000D-07  -6.253D-29 .                .              .   +          *
5.000D-07  -6.715D-29 .                .              .   +          *
6.000D-07  -7.156D-29 .                .              .   +          *
7.000D-07  -7.578D-29 .                .              .   +          *
8.000D-07  -7.982D-29 .                .              .   +          *
9.000D-07  -8.367D-29 .                .              .   +          *
1.000D-06  -8.736D-29 .                .              .   +          *
1.100D-06  -1.055D-01 .          + *   .              .              .
1.200D-06  -9.206D-02 .          +     .  *           .              .
1.300D-06  -8.340D-02 .          +     .     *        .              .
1.400D-06  -7.562D-02 .          +     .        *     .              .
1.500D-06  -6.526D-02 .          +     .           *  .              .
1.600D-06  -5.742D-02 .          +     .              *.              .
1.700D-06  -5.297D-02 .          +     .               *              .
1.800D-06  -4.652D-02 .          +     .              .*              .
1.900D-06  -3.917D-02 .          +     .              .   *           .
2.000D-06  -3.623D-02 .          +     .              .     *         .
2.100D-06  -3.360D-02 .          +     .              .       *       .
2.200D-06  -2.785D-02 .          +     .              .         *     .
2.300D-06  -2.415D-02 .          +     .              .           *   .
2.400D-06  -2.335D-02 .          +     .              .           *   .
2.500D-06  -2.020D-02 .          +     .              .             * .
2.600D-06  -1.584D-02 .          +     .              .               *.
2.700D-06  -1.545D-02 .          +     .              .               *.
2.800D-06  -1.512D-02 .          +     .              .               *.
2.900D-06  -1.146D-02 .          +     .              .                *.
3.000D-06  -9.559D-03 .          +     .              .                *.
3.100D-06  -1.029D-02 .          +     .              .                *.
3.200D-06  -8.556D-03 .          +     .              .                 *.
3.300D-06  -5.514D-03 .          +     .              .                 *.
3.400D-06  -6.350D-03 .          +     .              .                 *.
3.500D-06  -7.393D-03 .          +     .              .                 *.
```

JOB CONCLUDED
TOTAL JOB TIME 0.19

TRANSMISSION GATE WITH EK TRANSISTORS Figure 30

INPUT LISTING TEMPERATURE = 27.000 DEG C

****

```
*            FEEDTHROUGH ANALYSIS
*                C S BELL
*
VNWELL 1 2 DC 0
VSRC 2 0 DC 0
VGP 4 0 PULSE(1 -6.5 1E-6 1E-12 1E-12 2.5E-6 3.5E-6)
VGN 5 0 PULSE(-1 5  .6E-6 1E-12 1E-12 2.9E-6 3.5E-6)
VID 3 6 DC 0
M1 3 5 2 0 T280 L=80U W=80U NRS=.1 NRD=.1 AD=1280P AS=1280P PD=192U
+                           PS=192U
M2 3 4 2 1 T480 L=80U W=80U NRS=.1 NRD=.1 AD=1280P AS=1280P PD=192U
+                           PS=192U
C1 6 0 50P
R1 6 0 75K
 .MODEL T26 NMOS LAMBDA=.0175 UO=610 TPG=1 TOX=.0711U
+XJ=.5U NSUB=4.008E14 RSH=48.92 PB=.871 CGSO=2.91E-10
+CGDO=2.91E-10 CJ=1.77E-4 MJ=.5 CJSW=8.85E-11 MJSW=.3
+LD=.2U LEVEL=2 VTO=.53 GAMMA=.2232 NSS=4.758E11

 .MODEL T280 NMOS LAMBDA=.00155 UO=610 TPG=1 TOX=.0711U
+XJ=.5U NSUB=4.008E14 RSH=48.92 PB=.871 CGSO=2.91E-10
+CGDO=2.91E-10 CJ=1.77E-4 MJ=.5 CJSW=8.85E-11 MJSW=.3
+LD=.2U LEVEL=2 VTO=.604 GAMMA=.2509 NSS=4.983E11
+
 .MODEL T46 PMOS LAMBDA=.0275 UO=178 TPG=-1 TOX=.0711U
+XJ=.8U NSUB=3.7E16 RSH=285.6 PB=.719 CGSO=4.85E-10
+CGDO=4.85E-10 CJ=.958E-5 MJ=.5 CJSW=.958E-11 MJSW=.3
+LD=.6U LEVEL=2 VTO=-1.070 GAMMA=.6645 NSS=1.291E11
+
 .MODEL T480 PMOS LAMBDA=.00155 UO=178 TPG=-1 TOX=.0711U
+XJ=.8U NSUB=3.7E16 RSH=285.6 PB=.719 CGSO=4.85E-10
+CGDO=4.85E-10 CJ=.958E-5 MJ=.5 CJSW=.958E-11 MJSW=.3
+LD=.6U LEVEL=2 VTO=-1.009 GAMMA=.7736 NSS=1.478E11
 .WIDTH OUT=80
 .OPTION LIMPTS=1E6
 .TRAN 1E-7 3.5E-6
 .PLOT TRAN V(6) V(5) V(4)
 .END
```

TRANSMISSION GATE WITH EK TRANSISTORS Figure 30

MOSFET MODEL PARAMETERS TEMPERATURE = 27.000 DEG C

****

	T26	T280	T46	T480
TYPE	NMOS	NMOS	PMOS	PMOS
LEVEL	2.000	2.000	2.000	2.000
VTO	0.530	0.604	-1.070	-1.009
KP	2.96D-05	2.96D-05	8.65D-06	8.65D-06
GAMMA	0.223	0.251	0.665	0.774
PHI	0.529	0.529	0.763	0.763
LAMBDA	1.75D-02	1.55D-03	2.75D-02	1.55D-03
PB	0.871	0.871	0.719	0.719
CGSO	2.91D-10	2.91D-10	4.85D-10	4.85D-10
CGDO	2.91D-10	2.91D-10	4.85D-10	4.85D-10
RSH	48.920	48.920	285.600	285.600
CJ	1.77D-04	1.77D-04	9.58D-06	9.58D-06
MJ	0.500	0.500	0.500	0.500
CJSW	8.85D-11	8.85D-11	9.58D-12	9.58D-12
MJSW	0.300	0.300	0.300	0.300
TOX	7.11D-08	7.11D-08	7.11D-08	7.11D-08
NSUB	4.01D+14	4.01D+14	3.70D+16	3.70D+16
NSS	4.76D+11	4.98D+11	1.29D+11	1.48D+11
TPG	1.000	1.000	-1.000	-1.000
XJ	5.00D-07	5.00D-07	8.00D-07	8.00D-07
LD	2.00D-07	2.00D-07	6.00D-07	6.00D-07
UO	610.000	610.000	178.000	178.000

TRANSMISSION GATE WITH EK TRANSISTORS Figure 30

INITIAL TRANSIENT SOLUTION TEMPERATURE = 27.000 DEG C

****

NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE
(1)	0.0000	(2)	0.0000	(3)	0.0000	(4)	1.0000
(5)	-1.0000	(6)	0.0000				

VOLTAGE SOURCE CURRENTS

NAME	CURRENT
VNWELL	-2.230D-39
VSRC	-1.306D-39
VGP	0.000D+00
VGN	0.000D+00
VID	9.240D-40

TOTAL POWER DISSIPATION 0.00D+00 WATTS

*******06/21/86 ******** SPICE 2G.5 (10AUG81) ********10:39:02*****

TRANSMISSION GATE WITH EK TRANSISTORS Figure 30

OPERATING POINT INFORMATION TEMPERATURE = 27.000 DEG C

****

**** MOSFETS

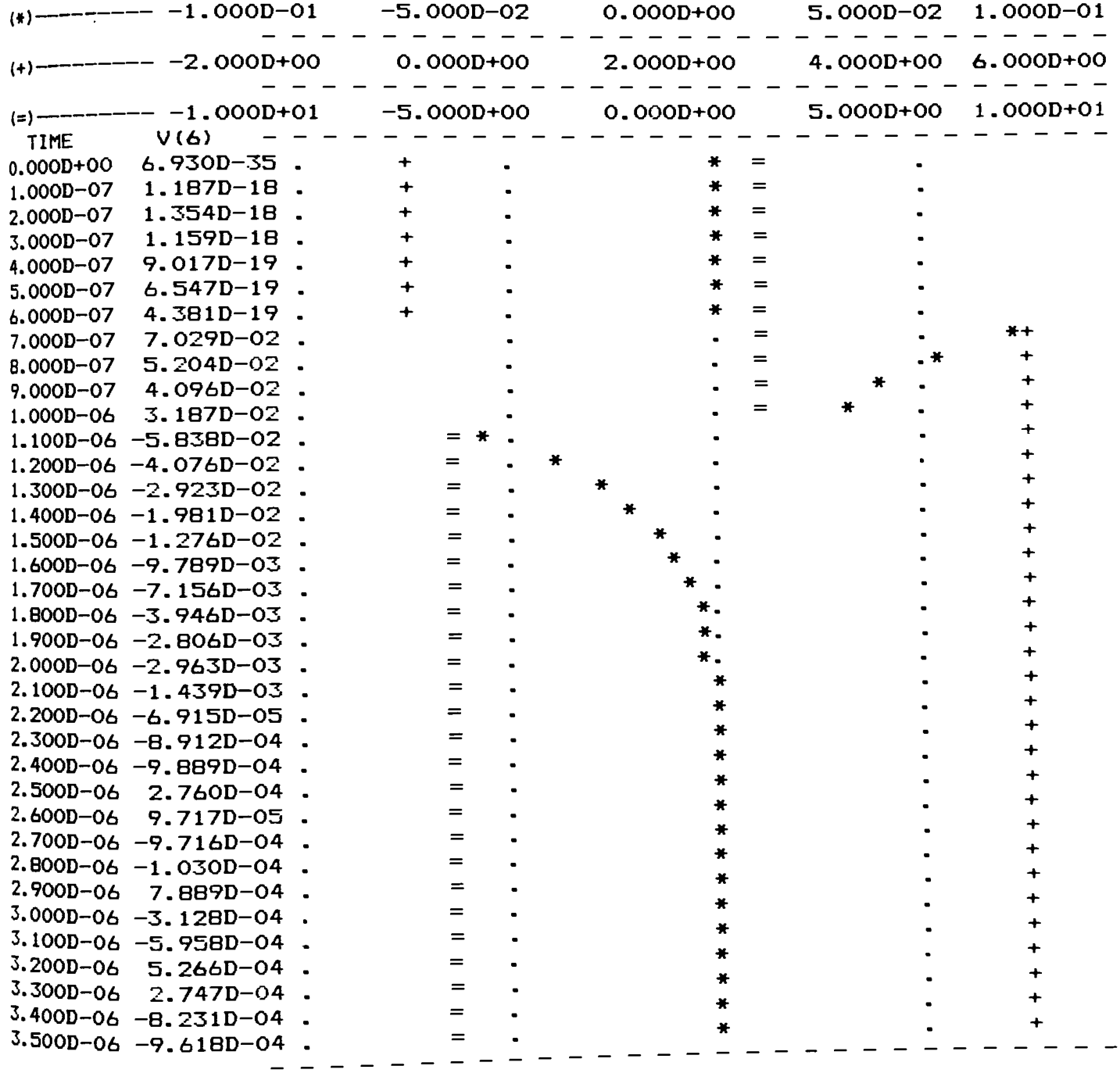
	M1	M2
MODEL	T280	T480
ID	0.00D+00	0.00D+00
VGS	-1.000	1.000
VDS	0.000	0.000
VBS	0.000	0.000

TRANSMISSION GATE WITH EK TRANSISTORS Figure 30

TRANSIENT ANALYSIS TEMPERATURE = 27.000 DEG C

****

LEGEND:
*: V(6)
+: V(5)
=: V(4)



TIME	V(6)
0.000D+00	6.930D-35
1.000D-07	1.187D-18
2.000D-07	1.354D-18
3.000D-07	1.159D-18
4.000D-07	9.017D-19
5.000D-07	6.547D-19
6.000D-07	4.381D-19
7.000D-07	7.029D-02
8.000D-07	5.204D-02
9.000D-07	4.096D-02
1.000D-06	3.187D-02
1.100D-06	-5.838D-02
1.200D-06	-4.076D-02
1.300D-06	-2.923D-02
1.400D-06	-1.981D-02
1.500D-06	-1.276D-02
1.600D-06	-9.789D-03
1.700D-06	-7.156D-03
1.800D-06	-3.946D-03
1.900D-06	-2.806D-03
2.000D-06	-2.963D-03
2.100D-06	-1.439D-03
2.200D-06	-6.915D-05
2.300D-06	-8.912D-04
2.400D-06	-9.889D-04
2.500D-06	2.760D-04
2.600D-06	9.717D-05
2.700D-06	-9.716D-04
2.800D-06	-1.030D-04
2.900D-06	7.889D-04
3.000D-06	-3.128D-04
3.100D-06	-5.958D-04
3.200D-06	5.266D-04
3.300D-06	2.747D-04
3.400D-06	-8.231D-04
3.500D-06	-9.618D-04

JOB CONCLUDED

TRANSMISSION GATE WITH EK TRANSISTORS Figure 31

INPUT LISTING TEMPERATURE = 27.000 DEG C

****

```
*            FEEDTHROUGH ANALYSIS
*                C S BELL
*
VNWELL 1 2 DC 0
VSRC 2 0 DC 0
VGP 4 0 PULSE(1 -6.5 1E-11 1E-12 1E-12 2.5E-6 3.5E-6)
VGN 5 0 PULSE(-1 5   1E-11 1E-12 1E-12 2.9E-6 3.5E-6)
VID 3 6 DC 0
M1 3 5 2 0 T280 L=80U W=80U NRS=.1 NRD=.1 AD=1280P AS=1280P PD=192U
+                           PS=192U
M2 3 4 2 1 T480 L=80U W=80U NRS=.1 NRD=.1 AD=1280P AS=1280P PD=192U
+                           PS=192U
C1 6 0 50P
R1 6 0 75K
 .MODEL T26 NMOS LAMBDA=.0175 UO=610 TPG=1 TOX=.0711U
+XJ=.5U NSUB=4.008E14 RSH=48.92 PB=.871 CGSO=2.91E-10
+CGDO=2.91E-10 CJ=1.77E-4 MJ=.5 CJSW=8.85E-11 MJSW=.3
+LD=.2U LEVEL=2 VTO=.53 GAMMA=.2232 NSS=4.758E11

 .MODEL T280 NMOS LAMBDA=.00155 UO=610 TPG=1 TOX=.0711U
+XJ=.5U NSUB=4.008E14 RSH=48.92 PB=.871 CGSO=2.91E-10
+CGDO=2.91E-10 CJ=1.77E-4 MJ=.5 CJSW=8.85E-11 MJSW=.3
+LD=.2U LEVEL=2 VTO=.604 GAMMA=.2509 NSS=4.983E11
+
 .MODEL T46 PMOS LAMBDA=.0275 UO=178 TPG=-1 TOX=.0711U
+XJ=.8U NSUB=3.7E16 RSH=285.6 PB=.719 CGSO=4.85E-10
+CGDO=4.85E-10 CJ=.958E-5 MJ=.5 CJSW=.958E-11 MJSW=.3
+LD=.6U LEVEL=2 VTO=-1.070 GAMMA=.6645 NSS=1.291E11
+
 .MODEL T480 PMOS LAMBDA=.00155 UO=178 TPG=-1 TOX=.0711U
+XJ=.8U NSUB=3.7E16 RSH=285.6 PB=.719 CGSO=4.85E-10
+CGDO=4.85E-10 CJ=.958E-5 MJ=.5 CJSW=.958E-11 MJSW=.3
+LD=.6U LEVEL=2 VTO=-1.009 GAMMA=.7736 NSS=1.478E11
 .WIDTH OUT=80
 .OPTION LIMPTS=1E6
 .TRAN 1E-11 4E-10
 .PLOT TRAN V(6) V(5) V(4)
 .END
```

TRANSMISSION GATE WITH EK TRANSISTORS Figure 31

MOSFET MODEL PARAMETERS TEMPERATURE = 27.000 DEG C

****

	T26	T280	T46	T480
TYPE	NMOS	NMOS	PMOS	PMOS
LEVEL	2.000	2.000	2.000	2.000
VTO	0.530	0.604	-1.070	-1.009
KP	2.96D-05	2.96D-05	8.65D-06	8.65D-06
GAMMA	0.223	0.251	0.665	0.774
PHI	0.529	0.529	0.763	0.763
LAMBDA	1.75D-02	1.55D-03	2.75D-02	1.55D-03
PB	0.871	0.871	0.719	0.719
CGSO	2.91D-10	2.91D-10	4.85D-10	4.85D-10
CGDO	2.91D-10	2.91D-10	4.85D-10	4.85D-10
RSH	48.920	48.920	285.600	285.600
CJ	1.77D-04	1.77D-04	9.58D-06	9.58D-06
MJ	0.500	0.500	0.500	0.500
CJSW	8.85D-11	8.85D-11	9.58D-12	9.58D-12
MJSW	0.300	0.300	0.300	0.300
TOX	7.11D-08	7.11D-08	7.11D-08	7.11D-08
NSUB	4.01D+14	4.01D+14	3.70D+16	3.70D+16
NSS	4.76D+11	4.98D+11	1.29D+11	1.48D+11
TPG	1.000	1.000	-1.000	-1.000
XJ	5.00D-07	5.00D-07	8.00D-07	8.00D-07
LD	2.00D-07	2.00D-07	6.00D-07	6.00D-07
UO	610.000	610.000	178.000	178.000

TRANSMISSION GATE WITH EK TRANSISTORS Figure 31

INITIAL TRANSIENT SOLUTION TEMPERATURE = 27.000 DEG C

NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE
(1)	0.0000	(2)	0.0000	(3)	0.0000	(4)	1.0000
(5)	-1.0000	(6)	0.0000				

VOLTAGE SOURCE CURRENTS

NAME	CURRENT
VNWELL	-2.230D-39
VSRC	-1.306D-39
VGP	0.000D+00
VGN	0.000D+00
VID	9.240D-40

TOTAL POWER DISSIPATION 0.00D+00 WATTS

*******06/21/86 ******** SPICE 2G.5 (10AUG81) ********10:42:08*****

TRANSMISSION GATE WITH EK TRANSISTORS Figure 31

OPERATING POINT INFORMATION TEMPERATURE = 27.000 DEG C

**** MOSFETS

	M1	M2
MODEL	T280	T480
ID	0.00D+00	0.00D+00
VGS	-1.000	1.000
VDS	0.000	0.000
VBS	0.000	0.000

TRANSMISSION GATE WITH EK TRANSISTORS Figure 31

TRANSIENT ANALYSIS TEMPERATURE = 27.000 DEG C

****

LEGEND:
*: V(6)
+: V(5)
=: V(4)

```
(*)---------- -2.000D-02      0.000D+00      2.000D-02      4.000D-02  6.000D-02
(+)---------- -2.000D+00      0.000D+00      2.000D+00      4.000D+00  6.000D+00
(=)---------- -1.000D+01     -5.000D+00      0.000D+00      5.000D+00  1.000D+01
  TIME        V(6)
0.000D+00   6.930D-35 .       +       *              .   =          .
1.000D-11   2.429D-19 .       +       *              .   =          .
2.000D-11   4.772D-02 .           =   .              .              .     * +
3.000D-11   5.159D-02 .           =   .              .              .      ++
4.000D-11   4.432D-02 .           =   .              .              .   *  +
5.000D-11   3.521D-02 .           =   .              .           *  .      +
6.000D-11   2.717D-02 .           =   .              .       *      .      +
7.000D-11   2.049D-02 .           =   .              *              .      +
8.000D-11   1.489D-02 .           =   .          *   .              .      +
9.000D-11   1.056D-02 .           =   .        *     .              .      +
1.000D-10   7.078D-03 .           =   .     *        .              .      +
1.100D-10   4.258D-03 .           =   .  *           .              .      +
1.200D-10   2.001D-03 .           =   .*             .              .      +
1.300D-10   2.619D-04 .           =   *              .              .      +
1.400D-10  -1.128D-03 .           =  *.              .              .      +
1.500D-10  -2.240D-03 .           = * .              .              .      +
1.600D-10  -3.129D-03 .           = * .              .              .      +
1.700D-10  -3.814D-03 .           =*  .              .              .      +
1.800D-10  -4.363D-03 .           =*  .              .              .      +
1.900D-10  -4.804D-03 .           =*  .              .              .      +
2.000D-10  -5.157D-03 .           X   .              .              .      +
2.100D-10  -5.430D-03 .           X   .              .              .      +
2.200D-10  -5.649D-03 .           X   .              .              .      +
2.300D-10  -5.825D-03 .           X   .              .              .      +
2.400D-10  -5.966D-03 .           X   .              .              .      +
2.500D-10  -6.075D-03 .           X   .              .              .      +
2.600D-10  -6.162D-03 .           X   .              .              .      +
2.700D-10  -6.233D-03 .           X   .              .              .      +
2.800D-10  -6.289D-03 .           X   .              .              .      +
2.900D-10  -6.333D-03 .           X   .              .              .      +
3.000D-10  -6.367D-03 .           X   .              .              .      +
3.100D-10  -6.395D-03 .           X   .              .              .      +
3.200D-10  -6.418D-03 .           X   .              .              .      +
3.300D-10  -6.435D-03 .          *=   .              .              .      +
3.400D-10  -6.449D-03 .          *=   .              .              .      +
3.500D-10  -6.460D-03 .          *=   .              .              .      +
3.600D-10  -6.469D-03 .          *=   .              .              .      +
3.700D-10  -6.476D-03 .          *=   .              .              .      +
3.800D-10  -6.481D-03 .          *=   .              .              .
```

```
3.900D-10 -6.485D-03 .        *=   .              .              .      +
4.000D-10 -6.489D-03 .        *=   .              .              .      +
          - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -

      JOB CONCLUDED
      TOTAL JOB TIME            0.53
```

TRANSMISSION GATE WITH EK TRANSISTORS Figure 32

INPUT LISTING TEMPERATURE = 27.000 DEG C

```
*            FEEDTHROUGH ANALYSIS
*                C S BELL
*
VNWELL 1 2 DC 0
VSRC 2 0 DC 0
VGP 4 0 PULSE(0  -6.0 .5E-9 2.10E-9 1E-10 2.5E-6 3.5E-6)
VGN 5 0 PULSE(-.4 5.6 .5E-9 2.25E-9 1E-10 2.5E-6 3.5E-6)
VID 3 6 DC 0
M1 3 5 2 0 T280 L=80U W=80U NRS=.1 NRD=.1 AD=1280P AS=1280P PD=192U
+                           PS=192U
M2 3 4 2 1 T480 L=80U W=80U NRS=.1 NRD=.1 AD=1280P AS=1280P PD=192U
+                           PS=192U
C1 6 0 50P
R1 6 0 75K
 .MODEL T26 NMOS LAMBDA=.0175 UO=610 TPG=1 TOX=.0711U
+XJ=.5U NSUB=4.008E14 RSH=48.92 PB=.871 CGSO=2.91E-10
+CGDO=2.91E-10 CJ=1.77E-4 MJ=.5 CJSW=8.85E-11 MJSW=.3
+LD=.2U LEVEL=2 VTO=.53 GAMMA=.2232 NSS=4.758E11

 .MODEL T280 NMOS LAMBDA=.00155 UO=610 TPG=1 TOX=.0711U
+XJ=.5U NSUB=4.008E14 RSH=48.92 PB=.871 CGSO=2.91E-10
+CGDO=2.91E-10 CJ=1.77E-4 MJ=.5 CJSW=8.85E-11 MJSW=.3
+LD=.2U LEVEL=2 VTO=.604 GAMMA=.2509 NSS=4.983E11
+
 .MODEL T46 PMOS LAMBDA=.0275 UO=178 TPG=-1 TOX=.0711U
+XJ=.8U NSUB=3.7E16 RSH=285.6 PB=.719 CGSO=4.85E-10
+CGDO=4.85E-10 CJ=.958E-5 MJ=.5 CJSW=.958E-11 MJSW=.3
+LD=.6U LEVEL=2 VTO=-1.070 GAMMA=.6645 NSS=1.291E11
+
 .MODEL T480 PMOS LAMBDA=.00155 UO=178 TPG=-1 TOX=.0711U
+XJ=.8U NSUB=3.7E16 RSH=285.6 PB=.719 CGSO=4.85E-10
+CGDO=4.85E-10 CJ=.958E-5 MJ=.5 CJSW=.958E-11 MJSW=.3
+LD=.6U LEVEL=2 VTO=-1.009 GAMMA=.7736 NSS=1.478E11
 .WIDTH OUT=80
 .OPTION LIMPTS=1E6
 .TRAN 5E-11 3E-9
 .PLOT TRAN V(6) V(5) V(4)
 .END
```

******06/21/86 ******** SPICE 2G.5 (10AUG81) ********10:46:41******

TRANSMISSION GATE WITH EK TRANSISTORS Figure 32

MOSFET MODEL PARAMETERS TEMPERATURE = 27.000 DEG C

****

	T26	T280	T46	T480
TYPE	NMOS	NMOS	PMOS	PMOS
LEVEL	2.000	2.000	2.000	2.000
VTO	0.530	0.604	-1.070	-1.009
KP	2.96D-05	2.96D-05	8.65D-06	8.65D-06
GAMMA	0.223	0.251	0.665	0.774
PHI	0.529	0.529	0.763	0.763
LAMBDA	1.75D-02	1.55D-03	2.75D-02	1.55D-03
PB	0.871	0.871	0.719	0.719
CGSO	2.91D-10	2.91D-10	4.85D-10	4.85D-10
CGDO	2.91D-10	2.91D-10	4.85D-10	4.85D-10
RSH	48.920	48.920	285.600	285.600
CJ	1.77D-04	1.77D-04	9.58D-06	9.58D-06
MJ	0.500	0.500	0.500	0.500
CJSW	8.85D-11	8.85D-11	9.58D-12	9.58D-12
MJSW	0.300	0.300	0.300	0.300
TOX	7.11D-08	7.11D-08	7.11D-08	7.11D-08
NSUB	4.01D+14	4.01D+14	3.70D+16	3.70D+16
NSS	4.76D+11	4.98D+11	1.29D+11	1.48D+11
TPG	1.000	1.000	-1.000	-1.000
XJ	5.00D-07	5.00D-07	8.00D-07	8.00D-07
LD	2.00D-07	2.00D-07	6.00D-07	6.00D-07
UO	610.000	610.000	178.000	178.000

TRANSMISSION GATE WITH EK TRANSISTORS Figure 32
INITIAL TRANSIENT SOLUTION TEMPERATURE = 27.000 DEG C

NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE
(1)	0.0000	(2)	0.0000	(3)	0.0000	(4)	0.0000
(5)	-0.4000	(6)	0.0000				

VOLTAGE SOURCE CURRENTS

NAME	CURRENT
VNWELL	-2.230D-39
VSRC	-1.306D-39
VGP	0.000D+00
VGN	0.000D+00
VID	9.240D-40

TOTAL POWER DISSIPATION 0.00D+00 WATTS

*******06/21/86 ******** SPICE 2G.5 (10AUG81) ********10:46:41*****

TRANSMISSION GATE WITH EK TRANSISTORS Figure 32

OPERATING POINT INFORMATION TEMPERATURE = 27.000 DEG C

**** MOSFETS

	M1	M2
MODEL	T2B0	T4B0
ID	0.00D+00	0.00D+00
VGS	-0.400	0.000
VDS	0.000	0.000
VBS	0.000	0.000

TRANSMISSION GATE WITH EK TRANSISTORS Figure 32

TRANSIENT ANALYSIS TEMPERATURE = 27.000 DEG C

****

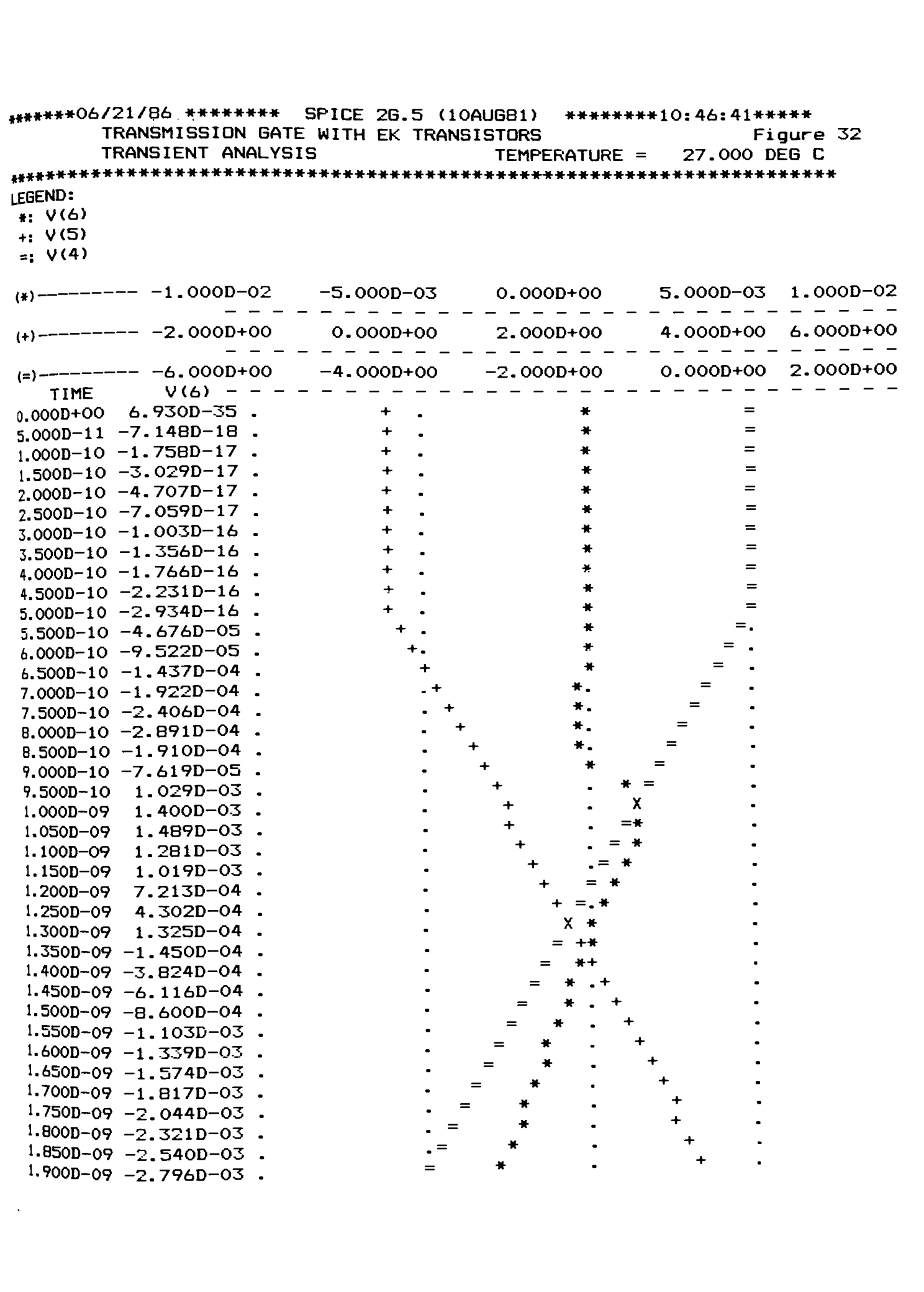
LEGEND:
*: V(6)
+: V(5)
=: V(4)

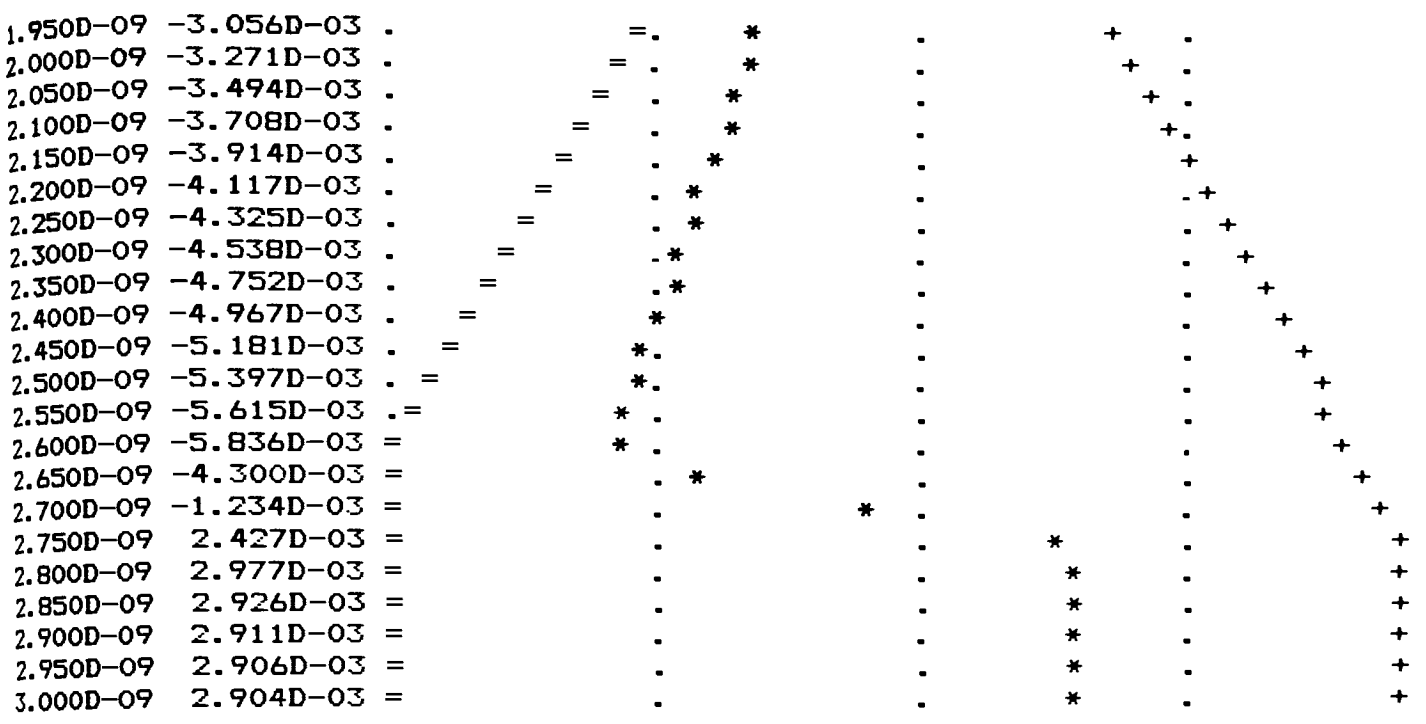
(*)--------- -1.000D-02 -5.000D-03 0.000D+00 5.000D-03 1.000D-02

(+)--------- -2.000D+00 0.000D+00 2.000D+00 4.000D+00 6.000D+00

(=)--------- -6.000D+00 -4.000D+00 -2.000D+00 0.000D+00 2.000D+00

TIME	V(6)
0.000D+00	6.930D-35
5.000D-11	-7.148D-18
1.000D-10	-1.758D-17
1.500D-10	-3.029D-17
2.000D-10	-4.707D-17
2.500D-10	-7.059D-17
3.000D-10	-1.003D-16
3.500D-10	-1.356D-16
4.000D-10	-1.766D-16
4.500D-10	-2.231D-16
5.000D-10	-2.934D-16
5.500D-10	-4.676D-05
6.000D-10	-9.522D-05
6.500D-10	-1.437D-04
7.000D-10	-1.922D-04
7.500D-10	-2.406D-04
8.000D-10	-2.891D-04
8.500D-10	-1.910D-04
9.000D-10	-7.619D-05
9.500D-10	1.029D-03
1.000D-09	1.400D-03
1.050D-09	1.489D-03
1.100D-09	1.281D-03
1.150D-09	1.019D-03
1.200D-09	7.213D-04
1.250D-09	4.302D-04
1.300D-09	1.325D-04
1.350D-09	-1.450D-04
1.400D-09	-3.824D-04
1.450D-09	-6.116D-04
1.500D-09	-8.600D-04
1.550D-09	-1.103D-03
1.600D-09	-1.339D-03
1.650D-09	-1.574D-03
1.700D-09	-1.817D-03
1.750D-09	-2.044D-03
1.800D-09	-2.321D-03
1.850D-09	-2.540D-03
1.900D-09	-2.796D-03





JOB CONCLUDED
TOTAL JOB TIME 1.36

TRANSMISSION GATE WITH EK TRANSISTORS Figure 33

INPUT LISTING TEMPERATURE = 27.000 DEG C

```
*            FEEDTHROUGH ANALYSIS
*                C S BELL
*
VNWELL 1 2 DC 0
VSRC 2 0 DC 0
VGP 4 0 PULSE(0  -6.0 .5E-9  2E-9 1E-10 2.5E-6 3.5E-6)
VGN 5 0 PULSE(-.4 5.6 .53E-9 2E-9 1E-10 2.5E-6 3.5E-6)
VID 3 6 DC 0
M1 3 5 2 0 T280 L=80U W=80U NRS=.1 NRD=.1 AD=1280P AS=1280P PD=192U
+                           PS=192U
M2 3 4 2 1 T480 L=80U W=80U NRS=.1 NRD=.1 AD=1280P AS=1280P PD=192U
+                           PS=192U
C1 6 0 50P
R1 6 0 75K
 .MODEL T26 NMOS LAMBDA=.0175 UO=610 TPG=1 TOX=.0711U
+XJ=.5U NSUB=4.008E14 RSH=48.92 PB=.871 CGSO=2.91E-10
+CGDO=2.91E-10 CJ=1.77E-4 MJ=.5 CJSW=8.85E-11 MJSW=.3
+LD=.2U LEVEL=2 VTO=.53 GAMMA=.2232 NSS=4.758E11

 .MODEL T280 NMOS LAMBDA=.00155 UO=610 TPG=1 TOX=.0711U
+XJ=.5U NSUB=4.008E14 RSH=48.92 PB=.871 CGSO=2.91E-10
+CGDO=2.91E-10 CJ=1.77E-4 MJ=.5 CJSW=8.85E-11 MJSW=.3
+LD=.2U LEVEL=2 VTO=.604 GAMMA=.2509 NSS=4.983E11
+
 .MODEL T46 PMOS LAMBDA=.0275 UO=178 TPG=-1 TOX=.0711U
+XJ=.8U NSUB=3.7E16 RSH=285.6 PB=.719 CGSO=4.85E-10
+CGDO=4.85E-10 CJ=.958E-5 MJ=.5 CJSW=.958E-11 MJSW=.3
+LD=.6U LEVEL=2 VTO=-1.070 GAMMA=.6645 NSS=1.291E11
+
 .MODEL T480 PMOS LAMBDA=.00155 UO=178 TPG=-1 TOX=.0711U
+XJ=.8U NSUB=3.7E16 RSH=285.6 PB=.719 CGSO=4.85E-10
+CGDO=4.85E-10 CJ=.958E-5 MJ=.5 CJSW=.958E-11 MJSW=.3
+LD=.6U LEVEL=2 VTO=-1.009 GAMMA=.7736 NSS=1.478E11
 .WIDTH OUT=80
 .OPTION LIMPTS=1E6
 .TRAN 5E-11 3E-9
 .PLOT TRAN V(6) V(5) V(4)
 .END
```

TRANSMISSION GATE WITH EK TRANSISTORS Figure 33

MOSFET MODEL PARAMETERS TEMPERATURE = 27.000 DEG C

****

	T26	T280	T46	T480
TYPE	NMOS	NMOS	PMOS	PMOS
LEVEL	2.000	2.000	2.000	2.000
VTO	0.530	0.604	-1.070	-1.009
KP	2.96D-05	2.96D-05	8.65D-06	8.65D-06
GAMMA	0.223	0.251	0.665	0.774
PHI	0.529	0.529	0.763	0.763
LAMBDA	1.75D-02	1.55D-03	2.75D-02	1.55D-03
PB	0.871	0.871	0.719	0.719
CGSO	2.91D-10	2.91D-10	4.85D-10	4.85D-10
CGDO	2.91D-10	2.91D-10	4.85D-10	4.85D-10
RSH	48.920	48.920	285.600	285.600
CJ	1.77D-04	1.77D-04	9.58D-06	9.58D-06
MJ	0.500	0.500	0.500	0.500
CJSW	8.85D-11	8.85D-11	9.58D-12	9.58D-12
MJSW	0.300	0.300	0.300	0.300
TOX	7.11D-08	7.11D-08	7.11D-08	7.11D-08
NSUB	4.01D+14	4.01D+14	3.70D+16	3.70D+16
NSS	4.76D+11	4.98D+11	1.29D+11	1.48D+11
TPG	1.000	1.000	-1.000	-1.000
XJ	5.00D-07	5.00D-07	8.00D-07	8.00D-07
LD	2.00D-07	2.00D-07	6.00D-07	6.00D-07
UO	610.000	610.000	178.000	178.000

*******06/21/86 ******** SPICE 2G.5 (10AUG81) *********10:49:58*****

TRANSMISSION GATE WITH EK TRANSISTORS Figure 33

INITIAL TRANSIENT SOLUTION TEMPERATURE = 27.000 DEG C

****

NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE
(1)	0.0000	(2)	0.0000	(3)	0.0000	(4)	0.0000
(5)	-0.4000	(6)	0.0000				

VOLTAGE SOURCE CURRENTS

NAME	CURRENT
VNWELL	-2.230D-39
VSRC	-1.306D-39
VGP	0.000D+00
VGN	0.000D+00
VID	9.240D-40

TOTAL POWER DISSIPATION 0.00D+00 WATTS

*******06/21/86 ******** SPICE 2G.5 (10AUG81) *********10:49:58*****

TRANSMISSION GATE WITH EK TRANSISTORS Figure 33

OPERATING POINT INFORMATION TEMPERATURE = 27.000 DEG C

****

**** MOSFETS

	M1	M2
MODEL	T280	T480
ID	0.00D+00	0.00D+00
VGS	-0.400	0.000
VDS	0.000	0.000
VBS	0.000	0.000

TRANSMISSION GATE WITH EK TRANSISTORS Figure 33

TRANSIENT ANALYSIS TEMPERATURE = 27.000 DEG C

****

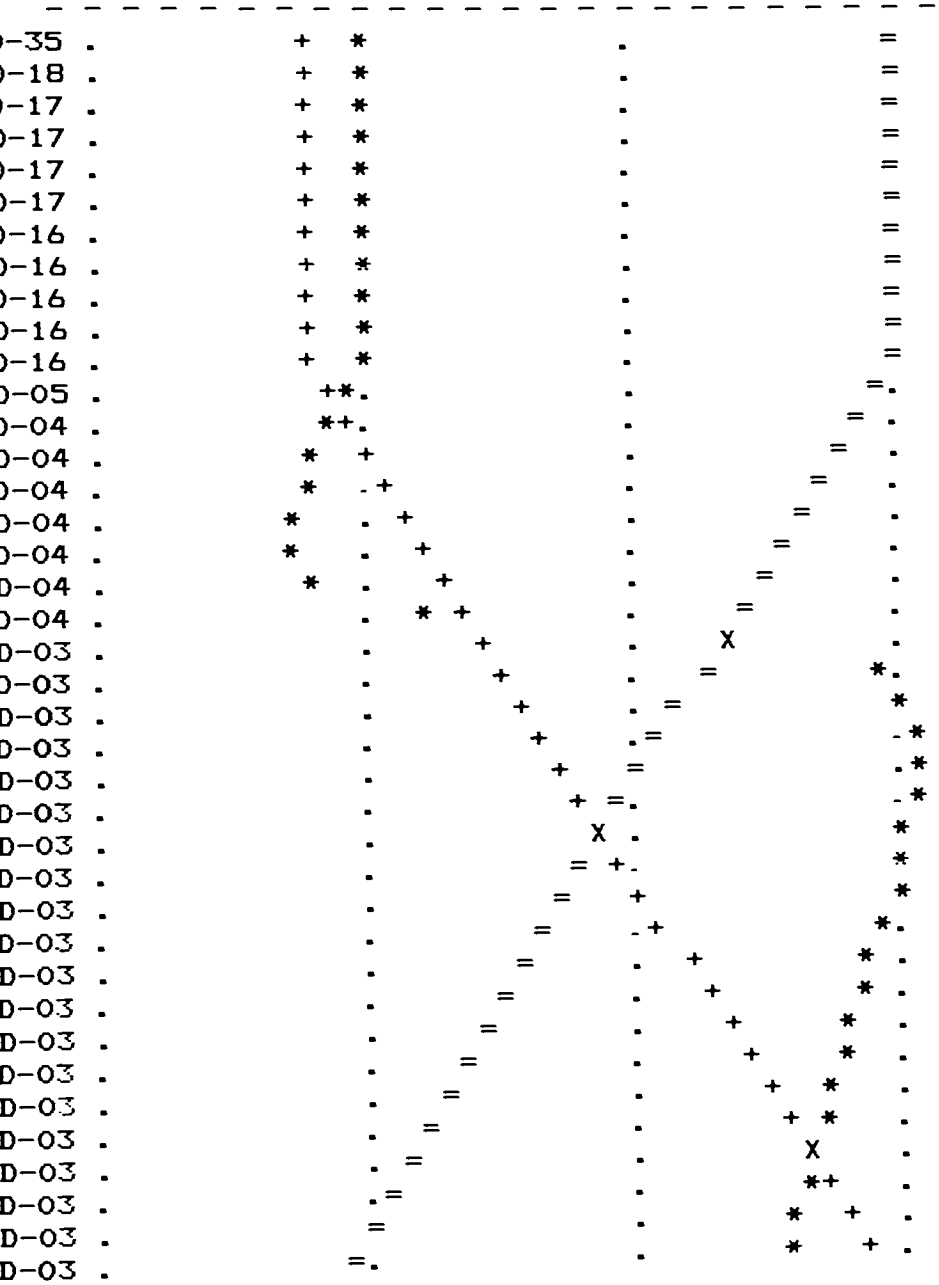
LEGEND:
*: V(6)
+: V(5)
=: V(4)

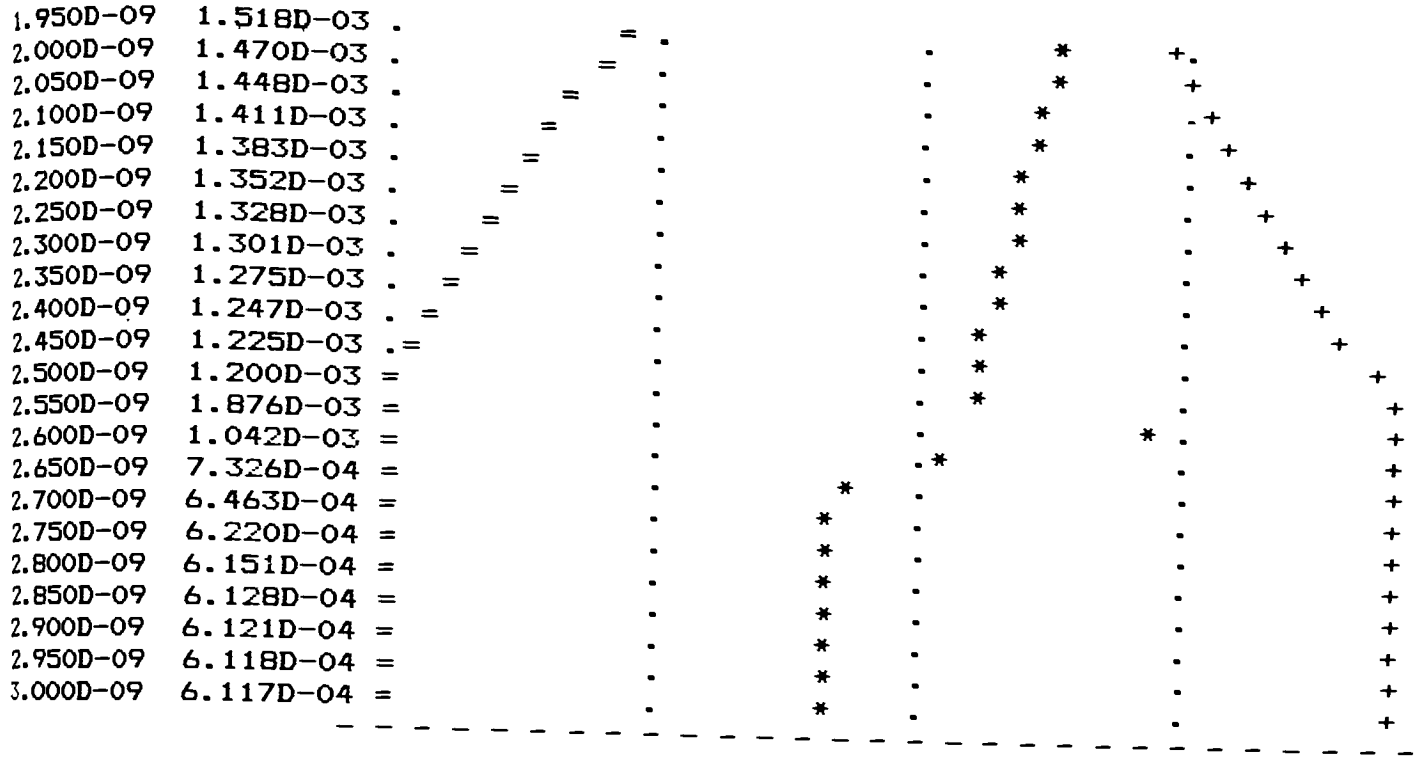
(*) -1.000D-03 0.000D+00 1.000D-03 2.000D-03 3.000D-03

(+) -2.000D+00 0.000D+00 2.000D+00 4.000D+00 6.000D+00

(=) -6.000D+00 -4.000D+00 -2.000D+00 0.000D+00 2.000D+00

TIME	V(6)
0.000D+00	6.930D-35
5.000D-11	-7.148D-18
1.000D-10	-1.758D-17
1.500D-10	-3.029D-17
2.000D-10	-4.707D-17
2.500D-10	-7.059D-17
3.000D-10	-1.003D-16
3.500D-10	-1.356D-16
4.000D-10	-1.766D-16
4.500D-10	-2.231D-16
5.000D-10	-2.934D-16
5.500D-10	-8.617D-05
6.000D-10	-1.324D-04
6.500D-10	-1.788D-04
7.000D-10	-2.250D-04
7.500D-10	-2.713D-04
8.000D-10	-2.676D-04
8.500D-10	-1.916D-04
9.000D-10	2.107D-04
9.500D-10	1.381D-03
1.000D-09	1.909D-03
1.050D-09	1.978D-03
1.100D-09	2.093D-03
1.150D-09	2.057D-03
1.200D-09	2.070D-03
1.250D-09	2.017D-03
1.300D-09	2.013D-03
1.350D-09	1.970D-03
1.400D-09	1.919D-03
1.450D-09	1.878D-03
1.500D-09	1.837D-03
1.550D-09	1.797D-03
1.600D-09	1.760D-03
1.650D-09	1.725D-03
1.700D-09	1.691D-03
1.750D-09	1.659D-03
1.800D-09	1.629D-03
1.850D-09	1.583D-03
1.900D-09	1.548D-03





JOB CONCLUDED
TOTAL JOB TIME 2.00

TRANSMISSION GATE WITH EK TRANSISTORS Figure 34

INPUT LISTING TEMPERATURE = 27.000 DEG C

```
*
*            FEEDTHROUGH ANALYSIS
*                C S BELL
*
VNWELL 1 2 DC 0
VSRC 2 0 DC 0
VGP 4 0 PULSE(0  -6.0 .5E-9  2E-9 1E-10 2.5E-6 3.5E-6)
VGN 5 0 PULSE(-.4 5.6 .54E-9 2E-9 1E-10 2.5E-6 3.5E-6)
VID 3 6 DC 0
M1 3 5 2 0 T280 L=80U W=80U NRS=.1 NRD=.1 AD=1280P AS=1280P PD=192U
+                           PS=192U
M2 3 4 2 1 T480 L=80U W=80U NRS=.1 NRD=.1 AD=1280P AS=1280P PD=192U
+                           PS=192U
C1 6 0 50P
R1 6 0 75K
 .MODEL T26 NMOS LAMBDA=.0175 UO=610 TPG=1 TOX=.0711U
+XJ=.5U NSUB=4.008E14 RSH=48.92 PB=.871 CGSO=2.91E-10
+CGDO=2.91E-10 CJ=1.77E-4 MJ=.5 CJSW=8.85E-11 MJSW=.3
+LD=.2U LEVEL=2 VTO=.53 GAMMA=.2232 NSS=4.758E11

 .MODEL T280 NMOS LAMBDA=.00155 UO=610 TPG=1 TOX=.0711U
+XJ=.5U NSUB=4.008E14 RSH=48.92 PB=.871 CGSO=2.91E-10
+CGDO=2.91E-10 CJ=1.77E-4 MJ=.5 CJSW=8.85E-11 MJSW=.3
+LD=.2U LEVEL=2 VTO=.604 GAMMA=.2509 NSS=4.983E11
+
 .MODEL T46 PMOS LAMBDA=.0275 UO=178 TPG=-1 TOX=.0711U
+XJ=.8U NSUB=3.7E16 RSH=285.6 PB=.719 CGSO=4.85E-10
+CGDO=4.85E-10 CJ=.958E-5 MJ=.5 CJSW=.958E-11 MJSW=.3
+LD=.6U LEVEL=2 VTO=-1.070 GAMMA=.6645 NSS=1.291E11
+
 .MODEL T480 PMOS LAMBDA=.00155 UO=178 TPG=-1 TOX=.0711U
+XJ=.8U NSUB=3.7E16 RSH=285.6 PB=.719 CGSO=4.85E-10
+CGDO=4.85E-10 CJ=.958E-5 MJ=.5 CJSW=.958E-11 MJSW=.3
+LD=.6U LEVEL=2 VTO=-1.009 GAMMA=.7736 NSS=1.478E11
 .WIDTH OUT=80
 .OPTION LIMPTS=1E6
 .TRAN 5E-11 3E-9
 .PLOT TRAN V(6) V(5) V(4)
 .END
```

TRANSMISSION GATE WITH EK TRANSISTORS Figure 34

MOSFET MODEL PARAMETERS TEMPERATURE = 27.000 DEG C

****

	T26	T280	T46	T480
TYPE	NMOS	NMOS	PMOS	PMOS
LEVEL	2.000	2.000	2.000	2.000
VTO	0.530	0.604	-1.070	-1.009
KP	2.96D-05	2.96D-05	8.65D-06	8.65D-06
GAMMA	0.223	0.251	0.665	0.774
PHI	0.529	0.529	0.763	0.763
LAMBDA	1.75D-02	1.55D-03	2.75D-02	1.55D-03
PB	0.871	0.871	0.719	0.719
CGSO	2.91D-10	2.91D-10	4.85D-10	4.85D-10
CGDO	2.91D-10	2.91D-10	4.85D-10	4.85D-10
RSH	48.920	48.920	285.600	285.600
CJ	1.77D-04	1.77D-04	9.58D-06	9.58D-06
MJ	0.500	0.500	0.500	0.500
CJSW	8.85D-11	8.85D-11	9.58D-12	9.58D-12
MJSW	0.300	0.300	0.300	0.300
TOX	7.11D-08	7.11D-08	7.11D-08	7.11D-08
NSUB	4.01D+14	4.01D+14	3.70D+16	3.70D+16
NSS	4.76D+11	4.98D+11	1.29D+11	1.48D+11
TPG	1.000	1.000	-1.000	-1.000
XJ	5.00D-07	5.00D-07	8.00D-07	8.00D-07
LD	2.00D-07	2.00D-07	6.00D-07	6.00D-07
UO	610.000	610.000	178.000	178.000

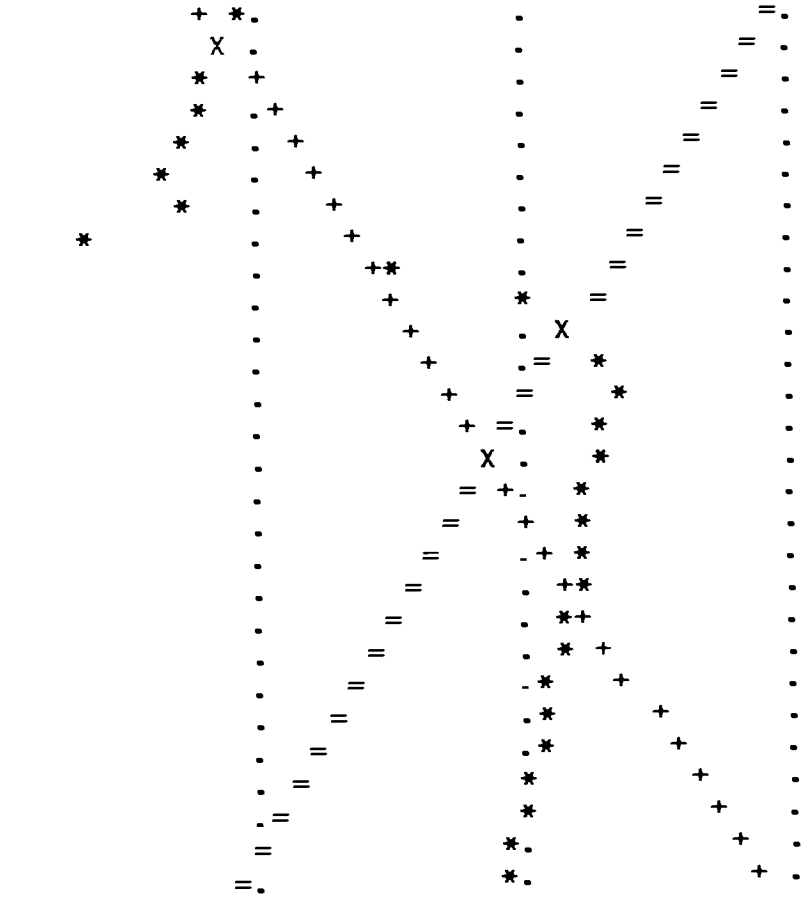
```
*****06/21/86 ********  SPICE 2G.5 (10AUG81)  ********10:52:25*****
        TRANSMISSION GATE WITH EK TRANSISTORS                    Figure 34
        INITIAL TRANSIENT SOLUTION       TEMPERATURE =   27.000 DEG C
*******************************************************************************

 NODE    VOLTAGE     NODE    VOLTAGE     NODE    VOLTAGE     NODE    VOLTAGE

(  1)     0.0000    (  2)     0.0000    (  3)     0.0000    (  4)     0.0000

(  5)    -0.4000    (  6)     0.0000


    VOLTAGE SOURCE CURRENTS

    NAME         CURRENT

    VNWELL    -2.230D-39
    VSRC      -1.306D-39
    VGP        0.000D+00
    VGN        0.000D+00
    VID        9.240D-40

    TOTAL POWER DISSIPATION   0.00D+00  WATTS
******06/21/86 ********  SPICE 2G.5 (10AUG81)  ********10:52:25*****
        TRANSMISSION GATE WITH EK TRANSISTORS                    Figure 34
        OPERATING POINT INFORMATION      TEMPERATURE =   27.000 DEG C
*******************************************************************************

**** MOSFETS

             M1          M2
MODEL      T280        T480
 ID         0.00D+00    0.00D+00
 VGS          -0.400       0.000
 VDS           0.000       0.000
 VBS           0.000       0.000
```

TRANSMISSION GATE WITH EK TRANSISTORS Figure 34
TRANSIENT ANALYSIS TEMPERATURE = 27.000 DEG C
****

LEGEND:
*: V(6)
+: V(5)
=: V(4)

```
(*)---------- -1.000D-03      0.000D+00      1.000D-03      2.000D-03  3.000D-03
(+)---------- -2.000D+00      0.000D+00      2.000D+00      4.000D+00  6.000D+00
(=)---------- -6.000D+00     -4.000D+00     -2.000D+00      0.000D+00  2.000D+00
```

TIME	V(6)
0.000D+00	6.930D-35
5.000D-11	-7.148D-18
1.000D-10	-1.758D-17
1.500D-10	-3.029D-17
2.000D-10	-4.707D-17
2.500D-10	-7.059D-17
3.000D-10	-1.003D-16
3.500D-10	-1.356D-16
4.000D-10	-1.766D-16
4.500D-10	-2.231D-16
5.000D-10	-2.934D-16
5.500D-10	-1.002D-04
6.000D-10	-1.464D-04
6.500D-10	-1.926D-04
7.000D-10	-2.389D-04
7.500D-10	-2.851D-04
8.000D-10	-3.300D-04
8.500D-10	-2.648D-04
9.000D-10	-6.191D-04
9.500D-10	4.806D-04
1.000D-09	1.024D-03
1.050D-09	1.165D-03
1.100D-09	1.284D-03
1.150D-09	1.337D-03
1.200D-09	1.315D-03
1.250D-09	1.283D-03
1.300D-09	1.240D-03
1.350D-09	1.206D-03
1.400D-09	1.188D-03
1.450D-09	1.186D-03
1.500D-09	1.139D-03
1.550D-09	1.107D-03
1.600D-09	1.091D-03
1.650D-09	1.057D-03
1.700D-09	1.039D-03
1.750D-09	1.008D-03
1.800D-09	9.901D-04
1.850D-09	9.626D-04
1.900D-09	9.340D-04



```
1.950D-09   9.167D-04 .                =  .                 *.                 +.
2.000D-09   8.901D-04 .               =   .                *  .               +
2.050D-09   8.735D-04 .             =     .                *  .              .+
2.100D-09   8.553D-04 .            =      .                *  .             .  +
2.150D-09   8.295D-04 .          =        .                *  .            .   +
2.200D-09   8.060D-04 .        =          .               *   .            .    +
2.250D-09   7.908D-04 .      =            .               *   .            .     +
2.300D-09   7.728D-04 .    =              .               *   .            .      +
2.350D-09   7.496D-04 .  =                .              *    .            .       +
2.400D-09   7.311D-04 . =                 .              *    .            .        +
2.450D-09   7.181D-04 .=                  .              *    .            .         +
2.500D-09   7.006D-04 =                   .              *    .            .          +
2.550D-09   2.073D-03 =                   .                   .            .*          +
2.600D-09   1.423D-03 =                   .                   .         *  .           +
2.650D-09   1.128D-03 =                   .                   .      *     .           +
2.700D-09   1.016D-03 =                   .                   *           .           +
2.750D-09   9.851D-04 =                   .                   *           .           +
2.800D-09   9.768D-04 =                   .                   *           .           +
2.850D-09   9.747D-04 =                   .                   *           .           +
2.900D-09   9.742D-04 =                   .                   *           .           +
2.950D-09   9.739D-04 =                   .                   *           .           +
3.000D-09   9.737D-04 =                   .                   *           .           +
                      - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -

 JOB CONCLUDED
 TOTAL JOB TIME            1.76
```

TRANSMISSION GATE WITH EK TRANSISTORS Figure 35

INPUT LISTING TEMPERATURE = 27.000 DEG C

****

```
*            FEEDTHROUGH ANALYSIS
*                C S BELL
*
VNWELL 1 2 DC 0
VSRC 2 0 DC 0
VGP 4 0 PULSE(0  -6.0 .5E-9  2E-9 1E-10 2.5E-6 3.5E-6)
VGN 5 0 PULSE(-.4 5.6 .55E-9 2E-9 1E-10 2.5E-6 3.5E-6)
VID 3 6 DC 0
M1 3 5 2 0 T280 L=80U W=80U NRS=.1 NRD=.1 AD=1280P AS=1280P PD=192U
+                           PS=192U
M2 3 4 2 1 T480 L=80U W=80U NRS=.1 NRD=.1 AD=1280P AS=1280P PD=192U
+                           PS=192U
C1 6 0 50P
R1 6 0 75K
 .MODEL T26 NMOS LAMBDA=.0175 UO=610 TPG=1 TOX=.0711U
+XJ=.5U NSUB=4.008E14 RSH=48.92 PB=.871 CGSO=2.91E-10
+CGDO=2.91E-10 CJ=1.77E-4 MJ=.5 CJSW=8.85E-11 MJSW=.3
+LD=.2U LEVEL=2 VTO=.53 GAMMA=.2232 NSS=4.758E11

 .MODEL T280 NMOS LAMBDA=.00155 UO=610 TPG=1 TOX=.0711U
+XJ=.5U NSUB=4.008E14 RSH=48.92 PB=.871 CGSO=2.91E-10
+CGDO=2.91E-10 CJ=1.77E-4 MJ=.5 CJSW=8.85E-11 MJSW=.3
+LD=.2U LEVEL=2 VTO=.604 GAMMA=.2509 NSS=4.983E11
+
 .MODEL T46 PMOS LAMBDA=.0275 UO=178 TPG=-1 TOX=.0711U
+XJ=.8U NSUB=3.7E16 RSH=285.6 PB=.719 CGSO=4.85E-10
+CGDO=4.85E-10 CJ=.958E-5 MJ=.5 CJSW=.958E-11 MJSW=.3
+LD=.6U LEVEL=2 VTO=-1.070 GAMMA=.6645 NSS=1.291E11
+
 .MODEL T480 PMOS LAMBDA=.00155 UO=178 TPG=-1 TOX=.0711U
+XJ=.8U NSUB=3.7E16 RSH=285.6 PB=.719 CGSO=4.85E-10
+CGDO=4.85E-10 CJ=.958E-5 MJ=.5 CJSW=.958E-11 MJSW=.3
+LD=.6U LEVEL=2 VTO=-1.009 GAMMA=.7736 NSS=1.478E11
 .WIDTH OUT=80
 .OPTION LIMPTS=1E6
 .TRAN 5E-11 3E-9
 .PLOT TRAN V(6) V(5) V(4)
 .END
```

TRANSMISSION GATE WITH EK TRANSISTORS Figure 35

MOSFET MODEL PARAMETERS TEMPERATURE = 27.000 DEG C

****

	T26	T280	T46	T480
TYPE	NMOS	NMOS	PMOS	PMOS
LEVEL	2.000	2.000	2.000	2.000
VTO	0.530	0.604	-1.070	-1.009
KP	2.96D-05	2.96D-05	8.65D-06	8.65D-06
GAMMA	0.223	0.251	0.665	0.774
PHI	0.529	0.529	0.763	0.763
LAMBDA	1.75D-02	1.55D-03	2.75D-02	1.55D-03
PB	0.871	0.871	0.719	0.719
CGSO	2.91D-10	2.91D-10	4.85D-10	4.85D-10
CGDO	2.91D-10	2.91D-10	4.85D-10	4.85D-10
RSH	48.920	48.920	285.600	285.600
CJ	1.77D-04	1.77D-04	9.58D-06	9.58D-06
MJ	0.500	0.500	0.500	0.500
CJSW	8.85D-11	8.85D-11	9.58D-12	9.58D-12
MJSW	0.300	0.300	0.300	0.300
TOX	7.11D-08	7.11D-08	7.11D-08	7.11D-08
NSUB	4.01D+14	4.01D+14	3.70D+16	3.70D+16
NSS	4.76D+11	4.98D+11	1.29D+11	1.48D+11
TPG	1.000	1.000	-1.000	-1.000
XJ	5.00D-07	5.00D-07	8.00D-07	8.00D-07
LD	2.00D-07	2.00D-07	6.00D-07	6.00D-07
UO	610.000	610.000	178.000	178.000

TRANSMISSION GATE WITH EK TRANSISTORS Figure 35

INITIAL TRANSIENT SOLUTION TEMPERATURE = 27.000 DEG C

****

NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE
(1)	0.0000	(2)	0.0000	(3)	0.0000	(4)	0.0000
(5)	-0.4000	(6)	0.0000				

VOLTAGE SOURCE CURRENTS

NAME	CURRENT
VNWELL	-2.230D-39
VSRC	-1.306D-39
VGP	0.000D+00
VGN	0.000D+00
VID	9.240D-40

TOTAL POWER DISSIPATION 0.00D+00 WATTS

*******06/21/86 ******** SPICE 2G.5 (10AUG81) ********10:54:40*****

TRANSMISSION GATE WITH EK TRANSISTORS Figure 35

OPERATING POINT INFORMATION TEMPERATURE = 27.000 DEG C

****

**** MOSFETS

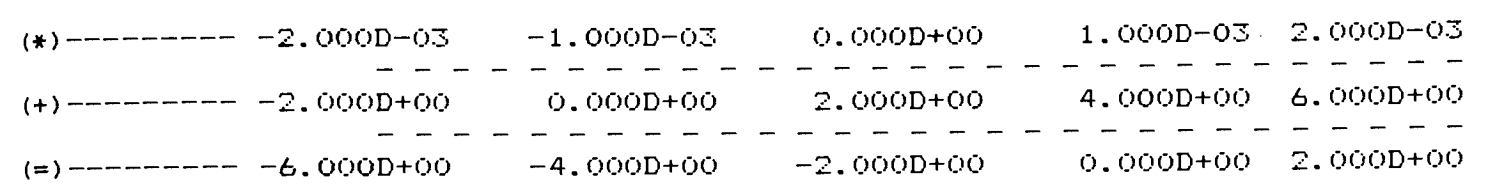
	M1	M2
MODEL	T280	T480
ID	0.00D+00	0.00D+00
VGS	-0.400	0.000
VDS	0.000	0.000
VBS	0.000	0.000

TRANSMISSION GATE WITH EK TRANSISTORS Figure 35

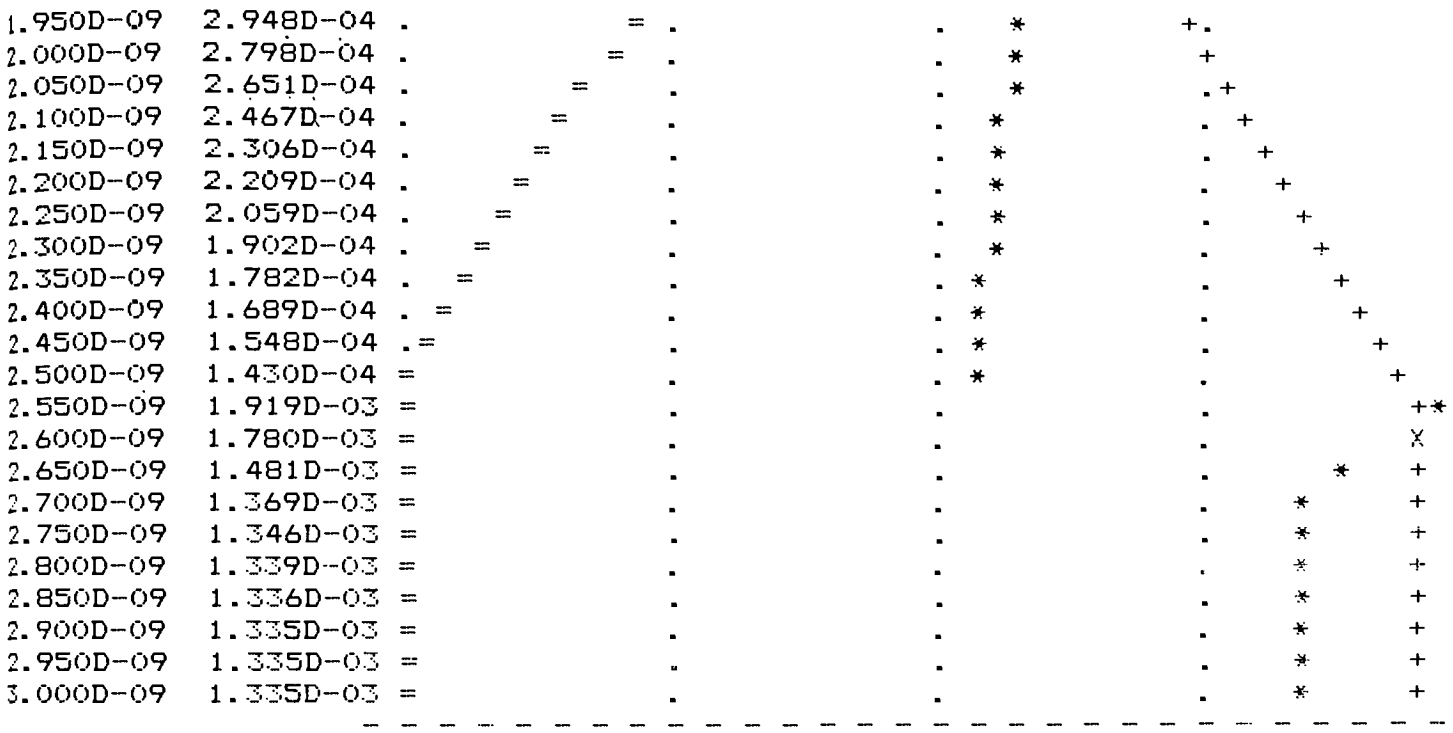
TRANSIENT ANALYSIS TEMPERATURE = 27.000 DEG C

****

LEGEND:
*: V(6)
+: V(5)
=: V(4)



TIME	V(6)
0.000D+00	6.930D-35
5.000D-11	-7.148D-18
1.000D-10	-1.758D-17
1.500D-10	-3.029D-17
2.000D-10	-4.707D-17
2.500D-10	-7.059D-17
3.000D-10	-1.003D-16
3.500D-10	-1.356D-16
4.000D-10	-1.766D-16
4.500D-10	-2.231D-16
5.000D-10	-2.934D-16
5.500D-10	-1.122D-04
6.000D-10	-1.603D-04
6.500D-10	-2.064D-04
7.000D-10	-2.529D-04
7.500D-10	-2.990D-04
8.000D-10	-3.455D-04
8.500D-10	-3.295D-04
9.000D-10	-1.484D-03
9.500D-10	-4.156D-04
1.000D-09	1.431D-04
1.050D-09	3.975D-04
1.100D-09	5.101D-04
1.150D-09	5.868D-04
1.200D-09	6.146D-04
1.250D-09	6.348D-04
1.300D-09	5.940D-04
1.350D-09	5.630D-04
1.400D-09	5.320D-04
1.450D-09	5.093D-04
1.500D-09	4.879D-04
1.550D-09	4.578D-04
1.600D-09	4.351D-04
1.650D-09	4.190D-04
1.700D-09	3.920D-04
1.750D-09	3.689D-04
1.800D-09	3.531D-04
1.850D-09	3.353D-04
1.900D-09	3.126D-04



JOB CONCLUDED
TOTAL JOB TIME 2.75